

Synopsys Announces Advanced Techniques In TSMC Reference Flow 8.0 to Address 45nm Design Challenges

Flow Includes Statistical Timing Analysis for Intra-die Variation, Automated DFM Hot-spot Fixing and New Dynamic Low-power Design Methodologies.

MOUNTAIN VIEW, Calif. and HSINCHU, Taiwan, June 4 [PRNewswire-FirstCall](#)/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, and Taiwan Semiconductor Manufacturing Company, Ltd. (TSE: 2330)(TSE: NYSE:) (TSE: TSM), today announced Synopsys support for TSMC's Reference Flow 8.0 and 45nm process technologies. Synopsys is supporting Reference Flow 8.0 in its Galaxy™ Design Platform, Discovery™ Verification Platform, and design for manufacturing (DFM) products.

TSMC Reference Flow 8.0 includes statistical timing analysis for intra-die variation, automated DFM hot-spot fixing and new dynamic low-power design methodologies. Advanced power management techniques include multi-voltage and MTCMOS power gating, as well as more commonly used techniques such as clock gating and multi-threshold, available through the Synopsys Galaxy Design Platform. Reference Flow 8.0 performs comprehensive dynamic and leakage power optimization and analysis throughout the synthesis, physical design and sign-off phases of the design process.

"Our design platforms' support of TSMC Reference Flow 8.0 enables designers to address complex, deep-submicron challenges," said Rich Goldman, vice president of Strategic Market Development at Synopsys. "Our continued relationship with TSMC provides our mutual customers with a comprehensive, low-risk solution from RTL to silicon."

The Synopsys Discovery Verification Platform enables power-aware simulation, formal equivalence checking, and static analysis of designs that use advanced power management techniques such as multiple power domains, level shifters, isolation cells, and retention memory elements. Advanced multi-voltage designs have been taped out with TSMC's manufacturing technology using Synopsys power management solutions.

"Through the years, Synopsys and TSMC have worked together to meet the evolving challenges of deep-submicron design," said Kuo Wu, deputy director of design service marketing at TSMC. "Manufacturing ease, yield, and leakage are vital design concerns at the 45-nanometer node. Synopsys tools and platforms address these concerns in TSMC Reference Flow 8.0."

Reference Flow 8.0 takes advantage of new capabilities available through the Galaxy Design Platform and PrimeYield design-yield analysis tool suite for 45nm readiness. For productivity gains during implementation, designers can use concurrent yield optimization for critical area reduction and automated hot-spot fixing within IC Compiler. For analysis, designers can now use PrimeYield LCC to perform parametric (timing) analysis in addition to functional hot-spot analysis. To enable this, the PrimeYield and Star-RCXT™ tools support advanced features such as Virtual CMP (VCMP) analysis engine.

Synopsys has worked with TSMC on a comprehensive variation-aware flow that allows designers to reduce margins, improve design robustness, and enhance parametric yield. The Synopsys variation-aware analysis solution consists of three important components: The Composite Current Source (CCS)-based statistical library, sensitivity-based extraction using the Star-RCXT VX tool and statistical timing analysis technology in the PrimeTime® VX tool. With uncertainties introduced by the wide variation in device and interconnect at the sub-45nm level, customers can apply this solution to their complex 45nm system-on-chip (SoC) designs today. Additional Synopsys enhancements featured in TSMC Reference Flow 8.0 include advanced design-for-test (DFT) capabilities and support of TSMC 45nm design rules.

About TSMC Reference Flow 8.0 Support

Reference Flow 8.0 incorporates comprehensive Synopsys-based RTL-to-GDSII solution using the Galaxy Design Platform for RTL synthesis, physical implementation and sign-off, and the Discovery™ Verification Platform with VCS®, HSPICE®, and HSIM®/Nanosim® for RTL verification and circuit simulation.

As an integral part of the reference flow, Galaxy support includes:

- Design Compiler® and Design Compiler topographical technology logic synthesis
- Power Compiler™ multi-voltage power management
- Leda® RTL Checker
- DFT MAX 1-pass test synthesis
- JupiterXT™ physical planning
- IC Compiler physical implementation
- PrimeTime, PrimeTime SI, and PrimeTime VX static timing and signal integrity sign-off

- PrimeRail power network sign-off
- PrimeTime PX full-chip power analysis
- Star-RCXT extraction
- Hercules™ PVS physical verification
- TetraMAX® automatic test pattern generation (ATPG)
- PrimeYield LCC for design-for-yield analysis

Synopsys Professional Services provides expertise in chip implementation and flow deployment with Reference Flow 8.0. Synopsys also distributes TSMC libraries through the DesignWare® Library.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at <https://www.synopsys.com/>.

About TSMC

TSMC is the world's largest dedicated semiconductor foundry, providing the industry's leading process technology and the foundry industry's largest portfolio of process-proven libraries, IP, design tools and reference flows. The Company's total managed capacity in 2006 exceeded seven million (8-inch equivalent) wafers, including capacity from two advanced 12-inch GigaFabs, four eight-inch fabs, one six-inch fab, as well as TSMC's wholly owned subsidiaries, WaferTech and TSMC (Shanghai), and its joint venture fab, SSMC. TSMC is the first foundry to provide 65nm production capabilities. Its corporate headquarters are in Hsinchu, Taiwan. For more information about TSMC please see <http://www.tsmc.com/>.

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