New Low Power Methodology Manual Demystifies Advanced Power Management

Springer Book Explains How to Ease Adoption of Aggressive Power Management Techniques

PR Newswire
NEW YORK, N.Y.

Springer Science+Business Media, LLC today announced the publication of the “Low Power Methodology Manual for System-on-Chip Design” (LPMM), a comprehensive and practical guide to managing both static (leakage) and dynamic power in system-on-chip (SoC) designs, critical to designers using 90-nanometer and below technology. Combining the authors’ extensive commercial experience, deep scientific understanding and silicon technology case studies, the LPMM demystifies the most effective new low power techniques with specific recommendations, and cautions against design pitfalls in a practical and easy-to-read style. Aggressive power management is now accessible to anyone designing or preparing to design SoCs with the latest intellectual property (IP) and electronic design automation (EDA) tools for low power mobile and consumer applications.

“We are thrilled to be able to bring this valuable book to professionals in the design automation sector and believe that it will be a helpful tool for those researching and implementing power reduction applications in the semiconductor industry and beyond,” said Alex Greene, Editorial Director of Engineering at Springer.

The LPMM authors are led by Michael Keating, Synopsys Fellow and principal author of the widely acclaimed “Reuse Methodology Manual for System-on-Chip Design,” now in a third edition, and David Flynn, ARM R&D Fellow and the original architect behind ARM’s synthesizable CPU family and the AMBA® on-chip interconnect standard. Keating and Flynn are joined by low power experts Alan Gibbons and Kaijian Shi of Synopsys and Robert Aitken, an ARM Fellow. The authors’ extensive commercial design and architecture experience covers systems, SoCs, and IP, as well as analog and mixed-signal circuits.

“By combining extensive commercial experience with silicon technology demonstrators, this manual offers documented practical methodologies that, in combination with new IP and tools, will enable designers to adopt advanced low-power techniques in their designs—particularly as the semiconductor industry migrates to the 65-nanometer node and beyond,” explained Mike Muller, Chief Technology Officer, ARM.

The LPMM covers a broad range of low power topics, beginning with a background and description of the basic approach to low power design. The LPMM then introduces clock gating and multiple threshold voltage (multi-Vt) methods, logic-level power reduction techniques, and multi-voltage design and architecture. It discusses power gating as well as dynamic voltage and frequency scaling, covering both RTL and architectural considerations for SoCs as well as silicon IP. One chapter is dedicated to implementation issues in low power design, including synthesis, place and route, timing analysis and power analysis. The book covers physical IP design considerations, including standard cells, memories and state retention for both flip-flops and memories. It also details the design of the power switching networks. Two appendices provide additional information including circuit design for sleep transistors and power switching networks.

In addition to the silicon technology case studies presented in the book, the authors have also produced an implementation Reference Methodology for the ARM1176JZF-S™ processor which employs the LPMM’s aggressive power-management techniques (see companion news release, ‘Synopsys and ARM optimize reference methodology for aggressive power management’).

The Low Power Methodology Manual (LPMM) is published in the Springer Series on Integrated Circuits and Systems, edited by

Professor Anantha Chandrakasan of the Massachusetts Institute of Technology. Professor Chandrakasan is a recognized leader in the area of low power design.
“Recognizing that managing power is critical to the success of modern electronics and that power management introduces significant challenges to the semiconductor design flow, the “Low Power Methodology Manual” demonstrates how the right combination of tools, IP and methodology can be used to address these challenges,” added John Chilton, Senior Vice President of Marketing and Strategic development at Synopsys. “The techniques described are both innovative and field-proven, and are presented in a format that is easy for the reader to follow and apply.”

The “Low Power Methodology Manual” will be launched at the Design Automation Conference (DAC)— the largest electronic design automation (EDA) conference with more than 10,000 attendees— June 4-8, 2007 in San Diego, CA. Copies of the LPMM will be on exhibit for review at the Springer booth (#3664), the Synopsys (Nasdaq:SNPS) Booth (#5278), and the ARM [(LSE:ARM); (Nasdaq:ARMHY)] booth (#4878). In addition, the authors will introduce the LPMM at the ARM-Synopsys low power luncheon (Wednesday, June 6th, 11:30AM, room 28ABCDE). Register to attend at http://synopsys.com/news/events/dac2007/arm_snps_lunch.html.

AvailabilityThe “Low Power Methodology Manual” will be available in August 2007 from Springer. For more information or to order the book online, please visit www.springer.com and search for Keating. More information on the book is available at http://www.lpmm-book.org.

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