Toshiba Standardizes on Synopsys IC Compiler With Release of Orion V1.0 Design Kit

IC Compiler is Key Enabler for More Than 20 Active/Completed Designs at Toshiba

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MOUNTAIN VIEW, Calif., May 29 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that Toshiba Corporation has completed the release of its Orion V1.0 design kit based on the Synopsys implementation toolset including the IC Compiler place-and-route solution. With this release, IC Compiler is now available to all designers at Toshiba, delivering increased productivity across the board as well as access to unique capabilities such as truly concurrent multi-corner/multi-mode (MCMM) optimization. IC Compiler also gives Toshiba designers a highly automated multi-voltage flow with tight correlation to other Synopsys technologies such as the PrimeTime® SI sign-off solution and Star-RCXT™ extraction solution. Since its first tapeout with IC Compiler in August 2006, Toshiba has successfully completed multiple designs at 130 and 90 nanometers (nm) and test designs at 65 nm. The very latest design is a high-performance, low-power media processor for mobile applications completed in April 2007.

"Our design teams focus on SoCs for digital consumer applications," said Takashi Yoshimori, technology executive of SoC Design, Semiconductor Company, Toshiba Corporation. "Multi-VDD techniques are essential to developing low-power ICs for these applications. By integrating low-power design automation and sign-off capability, IC Compiler enables us to successfully address these critical requirements by delivering excellent performance, as well as turnaround time improvement."

Toshiba has been an aggressive user of advanced capabilities in IC Compiler. Toshiba's designs often contain multiple operating modes, which benefit from IC Compiler's truly concurrent MCMM optimization that provides increased accuracy and faster time-to-results compared to other solutions relying on sequential approaches. All designs benefit from comprehensive leakage power management in IC Compiler as well as high-performance optimizations driven by IC Compiler's XPS (extended physical synthesis) technology.

The latest chip completed by Toshiba using IC Compiler is a 2-million-instance design comprised of multiple subsystems running at over 300 megahertz (MHz) with nested voltage levels. Achieving the combination of schedule, performance, low power and integrated functionality was an important achievement for Toshiba with this design targeting the hyper-competitive mobile phone market. IC Compiler's integration with the Galaxy™ Design Platform was a notable enabler in the development of this chip. This tight integration provides designers access to the latest technologies such as test compression using DFT MAX, strong link synthesis using Design Compiler® topographical technology, and tight correlation to the PrimeTime static timing analysis (STA) suite.

"We are fortunate to count a leader like Toshiba among the IC Compiler early adopters, helping us prove next-generation technologies on high-performance production designs," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "Toshiba standardizing on IC Compiler is a direct result of this long and fruitful relationship. We look forward to working with Toshiba to enable many more market-leading SoCs."

About IC Compiler

IC Compiler is Synopsys' next-generation place-and-route system. It provides superior results and faster time-to-results by extending physical synthesis to full place-and-route, and by enabling signoff-driven design closure. Current-generation solutions have a limited horizon because placement, clock tree, and routing are separate, disjointed operations. IC Compiler's Extended Physical Synthesis (XPS) technology breaks down the walls between these steps by extending physical synthesis to full place-and-route. IC Compiler has a unified, TCL-based architecture that implements innovations and harnesses some of the best Synopsys core technologies. It is a comprehensive place-and-route system with features necessary to implement next-generation designs, including physical synthesis, placement, routing, timing, signal integrity (SI) optimization, power reduction, design-for-test (DFT), and yield optimization.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market

for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

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