

# Synopsys IC Compiler Used By NEC Electronics for Tapeout of Gigahertz Processor

IC Compiler Helps NEC Electronics Achieve 2X Performance Improvement While Meeting Power Budget

PRNewswire-FirstCall  
MOUNTAIN VIEW, Calif.  
(NASDAQ:SNPS)

MOUNTAIN VIEW, Calif., May 29 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that NEC Electronics Corporation (TSE: 6723) has taped out its latest high-performance processor using Synopsys' IC Compiler next-generation place-and-route solution. Targeted at the high-end computer infrastructure market, this processor uses multiple cores operating at more than a gigahertz each, nearly double the speed of the previous version. IC Compiler, with its Extended Physical Synthesis (XPS) technology, played a critical role in achieving the gigahertz performance while keeping power dissipation in the range of a few microwatts per gate.

"We view IC Compiler's XPS technology as the natural evolution of physical synthesis pioneered by Synopsys," said Shinichi Iwamoto, associate vice president, Microcomputer Operations Unit, NEC Electronics. "We were able to adopt IC Compiler very easily and used it extensively during the prototyping phase of the design. IC Compiler's high accuracy gave our designers critical insight to fine-tune optimizations that helped us achieve our gigahertz performance target."

Used in conjunction with one of the most advanced RTL synthesis solutions, Design Compiler® topographical technology, IC Compiler boosted designer productivity by enabling a highly correlated flow between front-end design and physical implementation. IC Compiler's support for composite current source (CCS) models provided the accuracy necessary for this design by using current waveforms instead of delay and slew values to drive optimizations. Common technology such as cell delay and wire-delay calculation further improved productivity by enabling high correlation with Synopsys' industry standard PrimeTime® timing sign-off solution.

For leading-edge designs, particularly at gigahertz clock rates, power dissipation becomes a dominant constraint. IC Compiler's comprehensive support for leakage and dynamic power optimization allowed NEC Electronics to complete the design at the assigned budget.

"Very tight correlation between synthesis and physical implementation enables customers to minimize design time and achieve their aggressive performance goals," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "The combination of IC Compiler and Design Compiler topographical technology is increasingly the foundation for customers' standard design flows, delivering higher productivity and time-to-market benefits."

## About IC Compiler

IC Compiler is Synopsys' next-generation place-and-route system. It provides superior results and faster time-to-results by extending physical synthesis to full place-and-route, and by enabling signoff-driven design closure. Current-generation solutions have a limited horizon because placement, clock tree, and routing are separate, disjointed operations. IC Compiler's Extended Physical Synthesis (XPS) technology breaks down the walls between these steps by extending physical synthesis to full place-and-route. IC Compiler has a unified, TCL-based architecture that implements innovations and harnesses some of the best Synopsys core technologies. It is a comprehensive place-and-route system with the features necessary to implement next-generation designs, including physical synthesis, placement, routing, timing, signal integrity (SI) optimization, power reduction, design-for-test (DFT), and yield optimization.

## About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at <http://www.synopsys.com/>.

Synopsys, Design Compiler and PrimeTime are registered trademarks of Synopsys, Inc. Any other trademarks mentioned in this release are the intellectual property of their respective owners.

Synopsys, Inc.  
650-584-8635  
sgulizia@synopsys.com

Lisa Gillette-Martin  
MCA, Inc.  
650-968-8900 ext. 115  
lgmartin@mcapr.com

SOURCE: Synopsys, Inc.

CONTACT: Sheryl Gulizia of Synopsys, Inc., +1-650-584-8635, sgulizia@synopsys.com; or Lisa Gillette-Martin of MCA, Inc., +1-650-968-8900 ext. 115, lgmartin@mcapr.com, for Synopsys, Inc.

Web site: <http://www.synopsys.com/>

---