Synopsys Enhances DesignWare Synthesizable IP for AMBA 2 and AMBA 3 AXI Protocols

Increased Portfolio Breadth Helps Simplify Subsystem Integration

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MOUNTAIN VIEW, Calif., April 25 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced the 2007.04a release of DesignWare® synthesizable intellectual property (IP) for the ARM® AMBA® 2 and AMBA 3 AXI™ protocols. The DesignWare Library solution allows designers to easily integrate the high- speed protocol into their systems-on-chip (SoC) designs and enables designers of AMBA protocol-based systems to focus on the development of value-added elements to differentiate their products. The 2007.04a release includes a new I2S protocol IP for the APB bus, an AXI-to-APB3 compliant bridge with built-in fabric, and a highly configurable AXI-to-AXI bridge supporting a multi-layered AXI bus-based design. The release also includes extensive enhancements to the existing IP for the AMBA 2 and AMBA 3 AXI protocols.

The DesignWare IP for the I2S protocol implements the popular three-wire interface for streaming stereo audio between devices. This new IP removes the complexity of adopting the I2S protocol by offering a ready-to-implement, synthesizable IP. The AXI-to-APB3 bridge and fabric provides a seamless interface between the high-speed AXI bus and the APB3 peripheral bus. The AXI-to-APB3 bridge and fabric is backward-compatible with the APB 2.0 protocol and supports all existing APB-based peripherals. The AXI-to-AXI bridge provides upsizing, downsizing and multiple clock domain synchronization features between two AXI interconnects.

Additionally, the latest enhancement to the DesignWare interconnect fabric for AXI bridge includes bi-directional command support, solving the inherent master-to-slave communication paradox when two or more interconnects are connected together. The DesignWare interconnect fabric also helps designers meet their performance and area requirements by offering the choice of three timing configurations, providing users with the additional flexibility to optimize timing by trading off latency for clock rate.

The DesignWare solutions for AMBA interconnect include all three parts required to facilitate AMBA protocol-based subsystem designs: AMBA protocol- compliant synthesizable IP, AMBA 2 and AMBA 3 Assured™ Verification IP, and coreAssembler, an automated tool for rapidly assembling, configuring, and implementing AMBA 2 and AMBA 3 AXI protocol-based subsystems.

"We chose Synopsys' DesignWare Library because we needed an array of proven AMBA protocol-based IP for our latest design subsystem," said Andre Chartrand, vice president of engineering at Entropic Communications. "The DesignWare IP simplified subsystem integration, and its flexible configuration helped us meet our timing and area goals without sacrificing important features. In addition, Synopsys' comprehensive DesignWare library subscription model, which includes both synthesizable and verification IP, delivered a single vendor source for our design and verification team's needs."

"Quality IP availability and automation of subsystem assembly are key to reducing project design cycles," said John Koeter, senior director of marketing for the IP and Services Group at Synopsys. "The DesignWare solution for the AMBA protocol includes all the common, frequently used infrastructure building blocks, verification IP, and assembly tools, making it a comprehensive library of AMBA protocol-based IP. This portfolio of proven IP reduces risk and enables more predictable success for engineers implementing the popular AMBA protocol standard."

Availability

The 2007.04a release of DesignWare synthesizable IP for the AMBA 2 and AMBA 3 AXI protocols is available now at https://www.synopsys.com/designware-ip/soc-infrastructure-ip/amba.html . DesignWare Library licensees have access to this IP at no additional cost. RTL source code is available for license separately, on a pay-per-use basis.

About DesignWare Library

The DesignWare Library contains the principal intellectual property ingredients for design and verification including high-speed datapath components, AMBA (AMBA 2 & AMBA 3 AXI On-Chip Bus and peripherals), microcontrollers (8051, 6811) memory portfolio (memory controllers, memory BIST, memory building blocks, memory models), verification IP of standard bus and I/Os (PCI Express, PCI, PCI-X, USB 1.1, USB 2.0, USB On-The-Go, SATA, OCP, Ethernet, SIO, I2C), board verification IP and Foundry Libraries. All DesignWare Library elements are available under one license with no additional costs, per use fees, or royalties. For more information on DesignWare IP, visit: http://www.synopsys.com/designware/.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

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