Synopsys Design Compiler 2007 Boosts Designer Productivity and IC Performance

Topographical Technology Delivers Early Predictability for Designs Utilizing Advanced Low-Power and Test Techniques

MOUNTAIN VIEW, Calif., April 17 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced availability of the latest release of its Design Compiler® synthesis solution, Design Compiler 2007. The new release extends topographical technology to accelerate design closure for designs utilizing advanced low-power and test techniques, boosting designers productivity and IC performance. Topographical technology allows designers to accurately estimate a chip's power consumption during synthesis and address any power issues early in the design cycle. Moreover, topographical technology supports new test compression technology in Design Compiler 2007 to achieve high test quality while reducing test time and test data volume by more than 100 times.

"Using topographical technology, the performance predictions made by synthesis correlated within 5 percent of physical implementation results," said Huang Tao, design manager at Hisilicon. "Design Compiler 2007 additionally reduced chip area by an average of 5 percent while meeting the aggressive performance targets of our telecom designs. Superior performance complemented by tight correlation to layout is exactly what our designers need to bring competitive products to market faster."

Topographical technology delivers tight correlation between performance results seen during synthesis and what is achieved after layout. This eliminates the need for time-consuming iterations between RTL synthesis and physical layout to achieve design closure. Design Compiler shares technologies and infrastructure with the Galaxy™ Design Platform physical design solution to deliver a consistent and highly predictable RTL-to-GDSII path.

"We were faced with conflicting test goals at Cypress: we needed high test coverage but with very few dedicated test pins and limited memory on our legacy testers," said Don Smith, design director for the Data Communication Division at Cypress. "We evaluated Synopsys' adaptive-scan test compression technology, which took less than a day to adopt in our flow. Based on the results we've seen, we are confident that we can deliver the highest quality products while leveraging our existing test equipment infrastructure."

Design Compiler 2007 includes several innovative synthesis technologies such as adaptive retiming and power-driven clock gating, to deliver an average 8 percent higher performance, 4 percent smaller area and 5 percent lower power consumption compared to the previous release. In addition, the Synopsys Formality® equivalence checking solution has been enhanced to independently and thoroughly verify these technologies, thereby allowing designers to achieve higher performance without sacrificing verification.

"In today's design environment, each design presents a unique set of implementation challenges that must be overcome to ensure predictable silicon success," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "The advanced technologies in Design Compiler 2007 are helping designers meet their toughest performance targets while achieving the fastest and most predictable path to silicon."

About Design Compiler

The Design Compiler RTL synthesis solution encompasses advanced optimizations, complete low-power management, full design-for-test (DFT)/automatic test pattern generation (ATPG), seamless formal verification, and an extensive library of intellectual property (IP) components. Design Compiler 2007 is available immediately.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at https://www.synopsys.com/.

Synopsys, Design Compiler and Formality are registered trademarks of Synopsys, Inc. Galaxy is a trademark of Synopsys, Inc. Any other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

SOURCE: Synopsys, Inc.

CONTACT: Editorial, Sheryl Gulizia of Synopsys, Inc., +1-650-584-8635,
sgulizia@synopsys.com; or Rachel Modena Barasch, +1-650-325-7547,
rbarasch@mcapr.com

Web site: https://www.synopsys.com/