IC Compiler 2007 Release Continues Technology Innovation

35% Faster Runtime, Larger Capacity and Increased Automation Drive Designer Productivity

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MOUNTAIN VIEW, Calif., April 17 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced the 2007.03 release of IC Compiler, Synopsys' next-generation place-and-route solution. The 2007.03 release heralds significant advances in IC designer productivity through faster runtime, higher capacity, smarter multi-corner/multi-mode (MCMM) optimizations, and improved predictability. The release also rolls out physical design support for the emerging 45-nanometer (nm) technology wave. With greater than $100 million in cumulative customer orders and nearly 100 active customer designs, IC Compiler is increasingly the choice for market-leading IC designers in a broad class of applications and across a wide silicon technology spectrum.

"2007.03 is the most significant release of IC Compiler yet, delivering strong advantages for a large group of users," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "The release provides advances in core technology, benefiting users across the board. It also delivers improved productivity through higher automation in key functions such as MCMM optimizations and signoff-driven timing closure."

IC Compiler 2007.03 introduces new technology for the fastest operating mode which can deliver 35 percent runtime improvement without trading off quality-of-results. Coupled with improved capacity approaching 10 million gates on 16-gigabyte (GB) platforms, this new technology allows users to take on larger block partitions. The release adds early access to integrated hierarchical design planning, enabling users to efficiently tackle designs in the 100-million-gate range. Another key productivity-enhancing capability is the physical feasibility flow, which allows users to quickly generate and analyze multiple trial floorplans to determine the best starting point for detailed implementation.

For advanced designs, IC Compiler 2007.03 introduces Adaptive MCMM optimization technology, which delivers faster runtime and smaller memory utilization while providing the same level of accuracy. IC Compiler's approach to implementing truly concurrent optimization for designs with multiple modes and corners is an immense advantage for advanced users. These users cannot afford the scheduling impact of sequential optimization or accept the less-accurate merging technique employed by other place-and-route tools. The advanced designs also benefit from IC Compiler's signoff-driven timing closure which is now available as a production capability.

For emerging 45-nm designs, IC Compiler 2007.03 provides early support to leading-edge customers in the form of 45-nm placement and routing design rules. It also meets the new requirements for lithography compliance and chemical-mechanical polishing (CMP)-related metal uniformity. Today, Synopsys is partnering with major semiconductor vendors worldwide to ramp production support for 45-nm design implementation. As with 90-nm and 65-nm designs, Synopsys' physical implementation solution is the first in enabling tapeouts at 45-nm.

The IC Compiler 2007.03 release is available immediately.

About IC Compiler

IC Compiler is Synopsys' next-generation place-and-route system. It provides superior results and faster time-to-results by extending physical synthesis to full place-and-route, and by enabling signoff-driven design closure. Previous-generation solutions have a limited horizon because placement, clock tree, and routing are separate, disjointed operations. IC Compiler's Extended Physical Synthesis (XPS) technology breaks down the walls between these steps by extending physical synthesis to full place-and-route. IC Compiler has a unified, TCL-based architecture that implements innovations and harnesses some of the best Synopsys core technologies. It is a complete place-and-route system with everything necessary to implement next-generation designs, including physical synthesis, placement, routing, timing, signal integrity (SI) optimization, power reduction, design-for-test (DFT), and yield optimization.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

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