OCP-IP Standardizes on Synopsys' DesignWare Verification IP for OCP-IP's CoreCreator Verification Toolset

Collaboration Delivers OCP-Compliant Verification Solution for Improved Interoperability and Quality of OCP designs

MOUNTAIN VIEW, Calif. and BEAVERTON, Ore., April 10 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, and Open Core Protocol International Partnership (OCP-IP), an independent non-profit semiconductor industry consortium, today announced that they are collaborating to provide Synopsys' DesignWare® Verification IP (VIP) as part of OCP-IP's CoreCreator verification toolset. DesignWare VIP for OCP, part of Synopsys' portfolio of standards-based verification IP, will become the OCP-IP endorsed verification IP solution and will replace the OCP Bus Functional Models (BFM) currently provided with OCP's CoreCreator tool. The new, combined solution, which includes DesignWare VIP and CoreCreator's performance analysis, protocol checking, and transaction disassembly, gives OCP-IP members a common verification toolset, enabling maximum consistency and interoperability across OCP implementations. The collaboration also further expands OCP-IP's robust thriving infrastructure.

"The inclusion of Synopsys' DesignWare VIP into CoreCreator is a natural extension of the significant contributions already made by Synopsys to OCP- IP," said Ian Mackintosh, president of OCP-IP. "DesignWare VIP for OCP enables us to provide our members with a best-in-class verification solution that is current with latest versions of the standard, together with support for the latest verification methodologies."

The Synopsys DesignWare VIP for OCP will be available to OCP-IP members on request from the OCP-IP website as part of their subscription entitlement. Each release of the DesignWare VIP will be verified by OCP-IP for compliance to the latest version of the OCP standard. Synopsys' DesignWare VIP for OCP includes 100 percent coverage of the functional coverage groups defined in section 4 of the OCP-IP compliance check document.

Synopsys' DesignWare VIP for OCP supports Verilog, VHDL, and SystemVerilog testbenches and is fully compliant with the "Verification Methodology Manual" (VMM) guidelines for coverage-driven, constrained-random verification environments. It also supports the generation of trace files used by CoreCreator's OCP performance analysis, checker, and disassembly tools.

"When integrating IP in system-on-chip designs, one of the biggest challenges facing designers today is conformance to on-chip bus standards," said Ed Bard, senior director of IP marketing at Synopsys. "Verification IP plays an extremely important role in minimizing integration challenges by allowing designers to verify compliance of their interfaces. DesignWare VIP provides a consistent verification solution to the entire OCP-IP community, leading to maximized interoperability between OCP-IP member designs."

Availability

DesignWare Verification IP for OCP is available today and can be downloaded from the Synopsys IP directory: https://www.synopsys.com/verification/verification-ip.html . OCP-IP members will be able to obtain licenses of the DesignWare Verification IP for OCP within the second quarter of 2007 as part of their OCP-IP subscription. A separate announcement will be broadcast to OCP-IP members at that time.

About DesignWare Verification IP

DesignWare Verification IP is available in the DesignWare Library, the VCS® Verification Library, and as individual suites. The broad portfolio of design-proven, high quality, standards-based Verification IP (VIP), helps designers save testbench development time and reach functional coverage goals faster. It offers advanced functionality for block and chip-level verification and is an integral part of the Synopsys Discovery™ Verification Platform. The Verification IP supports all major simulators and enables customers to achieve up to five times faster verification when used with Synopsys VCS solution. The verification IP portfolio includes: AMBA 2.0, AMBA® 3 AXI™, OCP, PCI Express®, PCI-X®, PCI®, USB 1.1/2.0/OTG, 10/100/1G/10G Ethernet, I2C, SATA, Serial I/O, over 10,000 memory models and more. DesignWare Verification IP supports the Verification Methodology Manual which defines a reusable, consistent constrained random environment using a coverage-driven methodology to increase verification productivity and functional coverage.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia.

Visit Synopsys online at https://www.synopsys.com/.

About OCP-IP

The OCP International Partnership Association, Inc. (OCP-IP), formed in 2001, promotes and supports the Open Core Protocol (OCP) as the complete socket standard ensuring rapid creation and integration of interoperable virtual components. OCP-IP's Governing Steering Committee participants include: Nokia, Texas Instruments, Toshiba Semiconductor Group (including Toshiba America TAEC), and Sonics. OCP-IP is a non-profit corporation delivering the first fully supported, openly licensed, core-centric protocol comprehensively fulfilling system-level integration requirements. The OCP facilitates IP core reusability and reduces design time, risk, and manufacturing costs for SoC designs. VSIA endorses the OCP socket, and OCP-IP is affiliated with VSIA. For additional background and membership information, visit http://www.ocpip.org/.

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