Virage Logic Adds Liberty Composite Current Source Model Support to Memory and Logic IP

CCS Models Significantly Improve Accuracy for 65-nm and Below Semiconductor IP

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MOUNTAIN VIEW, Calif. and FREMONT, Calif., March 29 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software and Virage Logic Corporation (NASDAQ: VIRL), the semiconductor industry's trusted IP partner and pioneer in Silicon Aware IP™, today announced support of Composite Current Source (CCS) models for all advanced process node versions of Virage Logic's Self Test and Repair (STAR) Memory, Area, Speed and Power (ASAP) Memory™ and ASAP Logic™ Standard Cell product lines. Used in conjunction with the Synopsys Galaxy™ Design Platform, the high-accuracy CCS timing and noise models allow the designer to reduce guard-band margins during design implementation and sign-off, thus improving design performance and reducing design iterations. CCS models are proven to deliver sign-off level accuracy to within 2 percent of HSPICE® simulation as seen at leading semiconductor companies. Virage Logic will be presenting the details of its CCS-supported semiconductor intellectual property (IP) product portfolio as part of the CCS technology tutorial at the Synopsys Users' Group (SNUG) San Jose meeting on April 3.

"Customers look to Virage Logic for silicon-proven, high-quality semiconductor IP, particularly as they move to the advanced process geometries of 65 nanometers and below," said Ken Potts, vice president of product marketing at Virage Logic. "CCS models provide the accuracy and flexibility needed to model our advanced process technology memory and standard cell products to ensure our customers can proceed with confidence on their complex SoC designs."

CCS modeling technology, part of the open-source Liberty™ library modeling standard, enables highly accurate and comprehensive modeling of nanometer effects that encompass timing, signal integrity and power. CCS modeling technology is very adaptable, allowing for non-linear voltage or temperature scaling as well as the modeling of process variation. CCS models simplify advanced low-power design flows such as multi-Vt and multi-Vdd, as well as dynamic voltage and frequency scaling. There is significant industry- wide momentum behind CCS modeling technology with library availability from all leading IP vendors, foundries and integrated device manufacturers (IDMs).

"Our customers need world-class design implementation solutions coupled with high-accuracy, silicon-proven IP," said Bijan Kiani, vice president of marketing, Synopsys Implementation Group. "CCS-supported semiconductor IP from a leading provider such as Virage Logic used in conjunction with the Synopsys Galaxy Design Platform is a recipe for success for our mutual customers."

Availability

CCS timing and noise models are expected to be available for all Virage Logic's advanced process node products beginning in Q3 calendar 2007. For further information, please contact info@viragelogic.com .

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

About Virage Logic

Founded in 1996, Virage Logic Corporation rapidly established itself as a technology and market leader in providing advanced embedded memory intellectual property (IP) for the design of complex integrated circuits. Today, as the semiconductor industry's trusted IP partner, the company is a global leader in IP platforms comprising embedded memories, logic, and I/Os, and is pioneering the development of a new class of IP called Silicon Aware IP™. Silicon Aware IP tightly integrates Physical IP (memory, logic and I/Os) with the embedded test, diagnostic, and repair capabilities of Infrastructure IP to help ensure manufacturability and optimized yield at the advanced process nodes. Virage Logic's highly differentiated product portfolio provides higher performance, lower power, higher density and optimal yield to foundries, integrated device manufacturers (IDMs) and fabless customers who develop products for the consumer, communications and networking, hand-held and

portable, and computer and graphics markets. The company uses its FirstPass-Silicon™ Characterization Lab for certain products to help ensure high quality, reliable IP across a wide range of foundries and process technologies. The company also prides itself on providing superior customer support and was named the 2006 Customer Service Leader of the Year in the Semiconductor IP Market by Frost & Sullivan. Headquartered in Fremont, California, Virage Logic has R&D, sales and support offices worldwide.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including Synopsys' expectations of the date of availability of the CCS timing and noise models for Virage Logic's advanced process node products. These statements are based on current expectations and beliefs. Actual results could differ materially from these statements as a result of unforeseen difficulties in completing the commercial release of the solution, uncertainties attendant to any new product offering and certain statements contained in the section of Synopsys' Quarterly Report on Form 10-Q for the fiscal quarter ended January 31, 2007 entitled "Risk Factors."

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