STARC Deploys Synopsys Design Compiler Topographical Technology in New 65nm Methodology

Enhanced STARCAD-CEL Methodology Accelerates Time-to-Market for Major Japanese Semiconductor Companies

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that the Semiconductor Technology Academic Research Center (STARC) has deployed Synopsys Design Compiler® topographical technology in its 65- nanometer (nm) Synopsys Galaxy™ Design Platform-based design flow (project name: Eagle Flow) in the STARCAD®-CEL methodology. Topographical technology accurately predicts post-layout design performance such as timing, power, and area early in the design cycle, enabling designers to identify and fix issues during RTL synthesis. By helping to eliminate time-consuming iterations between RTL synthesis and physical layout to achieve design closure, topographical technology assists designers in closing on their performance goals quickly and more efficiently.

"Tight correlation between synthesis and layout is crucial to achieving design closure quickly and efficiently," said Nobuyuki Nishiguchi, vice president and general manager, Development Department-1 at STARC. "By implementing topographical technology in our 65nm design flow, we achieved an 11x improvement in turnaround time while meeting our stringent high-speed, low-power performance requirements. And, as part of the Galaxy Design Platform, topographical technology was very easy to adopt in the new STARCAD- CEL RTL-to-GDSII design methodology."

In addition to productivity improvements, the Galaxy Design Platform-based Eagle flow also supports a range of advanced capabilities addressing test, hierarchical clock planning, and low-power design. To achieve the 11x improvement over the previous-generation design flow, STARC introduced Design Compiler topographical technology into its STARCAD-CEL methodology which also includes IC Compiler for physical implementation, DFT MAX for test compression, the CCS library format for cell library modeling, and the golden PrimeTime® SI sign-off solution for timing.

Design Compiler topographical technology is an innovative, tapeout-proven synthesis technology that utilizes the Galaxy Design Platform physical implementation technologies to derive interconnect delays. This delay data allows the Design Compiler solution to predict post-layout design results such as timing, testability, and area during synthesis. Topographical technology also utilizes clock tree synthesis technology to estimate post-layout power consumption of the design.

"We are seeing very rapid adoption of Design Compiler topographical technology by customers worldwide because it can significantly improve their productivity," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "The majority of leading design houses in Japan utilize methodologies developed by STARC; now they can reap the benefits of using topographical technology as part of STARC's STARCAD-CEL release."

STARC is a research consortium of major Japanese semiconductor companies developing leading-edge system-on-chip (SoC) design methodologies.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at www.synopsys.com.

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