Synopsys Announces Low Power PHY IP for PCI Express, XAUI and SATA

Mixed -Signal IP Complements Synopsys' Market-Leading Portfolio of Serial Interface Controllers

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that it has expanded its DesignWare® Mixed-Signal intellectual property (MSIP) portfolio with new ultra low-power PCI Express®, XAUI and SATA physical layers (PHYs) in the 130- and 90-nanometer (nm) processes. These high-performance, mixed-signal PHYs offer highly differentiated, advanced built-in diagnostics for evaluating link performance and margin. When combined with the DesignWare digital controller cores and verification IP for PCIe and SATA protocols, the new PHY IP provides an optimized, lower risk, single vendor solution for designers incorporating these protocols in their system- on-chips (SoCs).

The new PHYs provide numerous benefits to the SoC designer, including compliance to the relevant standards specifications, the industry's smallest cores, low jitter and high receive sensitivity, resulting in a lower system bit error rate (BER) and a robust design with maximum margin and minimum power. The new solutions allow designers to significantly reduce power, requiring only 30 to 50 percent of the power consumption per lane of present solutions. These PHYs are based on an advanced analog architecture designed to scale to the next generation of data rates and process technologies as new high-speed SERDES protocols evolve.

Today design engineers developing SoCs for networking, storage, computing and consumer applications use PCIe, SATA and XAUI PHY's for high-speed interconnects operating at speeds from 1.25 gigabits per second (Gb/s) to 3.125 Gb/s. Testing links at these speeds, however, Synopsys' new PHYs incorporate advanced, built-in diagnostics -- accessible through JTAG (Joint Test Action Group) -- that are designed to replace traditional external loopback pass-fail testing with testing the link margin at speed. This approach is far superior because it allows designers to measure the eye- opening directly and verify the integrity of the signal, channel, and receiver while using only a conventional low-speed digital tester. This advanced approach reduces the total cost of ownership of the PHYs by providing excellent test coverage of the analog nature of high speed PHY's without using sophisticated high-cost test equipment. Support for Automated Test Equipment (ATE) is provided by delivering simple pass-fail JTAG vectors that ensure maximum test coverage when the PHYs are tested in production without the need for developing a complex test program.

"With the addition of the new PCIe, SATA and XAUI PHYs to its IP portfolio, Synopsys clearly demonstrates its commitment to delivering low- power, high-performance interconnects," said Jag Bolaria Senior Analyst at The Linley Group. "These new PHYs are very low in power consumption and include advanced features such on-board diagnostics and ATE."

"The release of the new PHYs firmly establishes our leadership in Mixed- Signal IP and in complete solutions for PCIe, SATA and XAUI. We are now targeting the next generation of high-speed, high-performance serial interconnects," said Guri Stark, vice president of Marketing, Synopsys' Solutions Group.

Availability

The DesignWare SATA and XAUI PHYs are currently available in limited production for 130- and 90-nm process technologies. The DesignWare PHY for PCI Express is available now for volume production.

About DesignWare Mixed Signal IP

Synopsys enables designers to quickly integrate analog mixed signal IP (MSIP) into next-generation SoCs by offering a comprehensive portfolio of high performance PHY IP for the PCI Express, SATA, XAUI and USB protocols. Available for industry-leading processes, the DesignWare Mixed Signal IP portfolio meets the needs of today's high-speed SoC designs for the networking, storage, computing, and consumer electronics markets. The DesignWare MSIP offering is complemented by a comprehensive suite of digital controllers and verification IP to provide chip developers with a complete solution for SoC integration. Each MSIP can be licensed individually, on a fee-per-project basis or users can opt for the Volume Purchase Agreement, which enables them to license all the MSIP in one simple agreement. For more information on DesignWare MSIP, visit: www.synopsys.com/designware

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market,

enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at www.synopsys.com

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