Synopsys and Virtio to Connect Hardware and Software Development Flows With Advanced ESL Solution

Integration of Synopsys System Studio and Virtio Software Models to Reduce SoC Design Cycle; Synopsys Makes Equity Investment in Virtio

Synopsys, Inc. (NASDAQ: SNPS), the world leader in semiconductor design software, and Virtio, a leading provider of Virtual Platforms for embedded software development, today announced that the companies are collaborating on a comprehensive electronic system level (ESL) solution that connects hardware and software development flows for leading system-on-chip (SoC) platforms. Under the collaboration, Virtio and Synopsys will integrate Virtio's high-speed software models for advanced SoC platforms, including models for popular embedded processors, with Synopsys' best-in-class, system-to-RTL verification solutions in the Discovery™ Verification Platform. This integrated, ESL verification solution is unique in that it will enable the concurrent development and verification of hardware and software throughout the design cycle, resulting in significantly faster releases of platform-based SoC products. The parties also announced that Synopsys has made an equity investment in Virtio.

"Up to this point, architecture models and pre-silicon software platform models have been developed independently from each other," said Paul Werp, director of marketing, Cellular Systems Software at Texas Instruments. "The Virtio-Synopsys collaboration will help ensure shortened, predictable design cycles and help us deliver trusted, pre-silicon software development models to our customers six to nine months earlier."

Connecting Hardware and Software Development Flows

Virtio's Virtual Platform software models provide engineers with high-speed, pre-silicon software execution environments that allow them to develop SoC-related software before hardware is available. The integration of Virtio's Virtual Platforms with the Synopsys System Studio system-level design environment will enable engineers to concurrently develop and verify SoC software and hardware, with the confidence that the software is fully compatible with the final hardware. The integration of System Studio with the Synopsys VCS® RTL verification solution and the Vera® testbench automation tool provides a unified system-to-RTL verification environment that combined with Virtio's solution will ensure that virtual software platform models, architecture models, and RTL models stay mutually consistent. The result will be a predictable, concurrent hardware and software development flow that substantially reduces the product design cycle and lowers project risk.

"We have been working very closely with major SoC platform providers to move software development up in the design process," said Shay Ben-Chorin, CEO at Virtio. "This collaboration provides the critical integration between Virtio's pre-silicon software development environment and Synopsys' comprehensive system-to-RTL verification solution, ensuring consistency between the hardware and software representation for a specific SoC platform."

Software Content Needs Earlier Verification

The increasing software content in today's advanced SoC platforms requires a concurrent development flow spanning hardware and software. The result is the need to start software development and verification well in advance of hardware delivery to ensure the timely availability of software components. The key challenge is to ensure that an accurate, high-speed software execution environment is available early in the project, and that it stays consistent with the evolving architecture and hardware design during the course of the development process.

"SoC embedded software development is becoming a critical factor for the timely availability of our customers' products," said Manoj Gandhi, senior vice president and general manager, Verification Group at Synopsys, Inc. "Our collaboration with Virtio addresses our customers' need for a concurrent software and hardware development flow. We have invested in Virtio because of its impressive technology, SoC platform partners, its leading customers, and our ongoing commitment to providing our customers with comprehensive SoC design and verification solutions."

Availability

The integrated Synopsys-Virtio solution will be available for early customers in the third quarter of calendar 2004. General availability will begin in the fourth quarter of calendar 2004.

About Virtio

Virtio speeds the creation and distribution of software models of embedded systems for early software development and integration. These software models, called Virtual Platforms, help embedded system suppliers and developers shorten the design cycle and break down critical time-to-market barriers. Many Virtual Platforms are available prior to the hardware to significantly shorten hardware/software integration. Virtio is based in Campbell, California in the U.S.A with development

centers in Campbell and the Alba Centre, Livingston, Scotland. Additional information about Virtio is available at http://www.virtio.com/.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is the world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has offices in more than 60 locations located throughout North America, Europe, Japan and Asia. Visit Synopsys online at https://www.synopsys.com/.

Forward Looking Statements

This press release contains forward-looking statements within the meaning of the safe harbor provisions of Section 21E of the Securities Exchange Act of 1934, including statements regarding the dates of availability and expected benefits of the Synopsys-Virtio integrated solution. These statements are based on Synopsys' and Virtio's current expectations and beliefs. Actual results could differ materially from the results implied by these statements as a result of unforeseen difficulties in completing integration of Synopsys' System Studio system-level design environment, VCS RTL verification tool, and Vera testbench automation tool with Virtio's high-speed, pre-silicon software execution environment for leading SoC platforms, as well as other factors contained in Synopsys' Quarterly Report on Form 10-Q filed with the Securities and Exchange Commission on June 10, 2004 under the caption "Factors That May Affect Future Results."

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SOURCE: Synopsys, Inc.

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