Cypress Deploys Synopsys PrimeRail to Speed Tapeout of Mobile Phone IC Design

Synopsys Galaxy Design Platform and PrimeRail Deliver Complete Flow for Multi-threshold CMOS Design

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that Cypress Semiconductor Corp. has successfully taped out its West Bridge™ Antioch™ peripheral controller multimedia 3G/3.5G mobile phone integrated circuit (IC) using the Synopsys Galaxy™ design platform RTL-to- GDSII low-power solution, including the PrimeRail dynamic power network analysis solution. The multithreshold CMOS (MTCMOS) power gating feature in the Galaxy design platform enabled Cypress to complete its ultra-low-power design with world-class performance and optimized standby current. PrimeRail, a key component of the Galaxy design platform, enabled peak current analysis for the multiple power domains of the Power Gating-based design during physical implementation.

"For our mobile phone chip design, we needed a solution that could address peak current problems related to the use of Power Gating switches," said Nagendra Cherukupalli, vice president of Asia Pacific design centers and chip integration at Cypress. "Synopsys' PrimeRail and its integration with the Galaxy design platform enabled our designers to analyze power integrity issues of the power gating switches and decoupling capacitors prior to tapeout."

Built on Synopsys' gold-standard Star-RCXT™ extraction and PrimeTime® sign-off technologies, PrimeRail offers full-chip analysis, dynamic memory and macro-modeling capabilities for advanced multi-voltage, low-power, high- performance designs. Its multimode analysis capability enables users to pinpoint and mitigate problems with critical power-up rush current or excessive current during wake-up to active mode in MTCMOS designs. PrimeRail is integrated with the Galaxy design platform, allowing designers to predict voltage drop during floorplanning, perform pre- and post-layout analysis with on-chip decoupling capacitance, and achieve full-chip sign-off with package parasitics.

"Cypress has once again placed their confidence in Synopsys' comprehensive low-power solution," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "PrimeRail's analysis capabilities are an extension of our low-power leadership, and the power network solution is the latest in our efforts to constantly strengthen Synopsys offerings. The Cypress project demonstrates our commitment to addressing the growing challenges designers face with low-power design, particularly in the areas of mobile and wireless applications."

Cypress is a leader in high-performance silicon solutions for consumer, computation, and data communications applications.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at www.synopsys.com .

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