Synopsys Sets the Stage for Another Significant Interoperability Initiative at the 17th EDA Interoperability Developers' Forum

Sun Microsystems Executive to Present Keynote

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that the 17th electronic design automation (EDA) Interoperability Developers' Forum will be held on May 17, 2006 in Santa Clara, CA. Since its inception in 1998, this open forum has featured many interoperability announcements, presentations and discussions. The current event continues this tradition by introducing a new interoperability initiative in the development of the seminal open source Liberty® library format. Furthermore, the Forum will feature presentations from Synopsys, other EDA vendors, standards luminaries and designers on the latest innovations in EDA initiatives, standards, open source formats and databases.

Sunil Joshi, senior vice president of Design Tools, Performance and Quality Technologies in Sun® Microsystems' Scalable Systems Group, will present the keynote address "Opening The Doors to Hardware Innovation." In his address, Joshi will discuss the challenges of changing market dynamics and present some of the opportunities created by open source hardware such as OpenSPARC®.

"The EDA Interoperability Forum has established itself as a great venue for chip designers and EDA vendors to discuss open interfaces and open source software. However, open source standards are no longer confined to simply software," said Sunil Joshi. "The open sourcing of the state-of-the-art, 64-bit, 32-thread OpenSPARC UltraSPARC T1 processor at the RTL level signals a new era for the hardware designer. Now designers can leverage this architecture in conjunction with the open standards in the EDA industry to increase design efficiencies and speed time-to-market."

The forum will feature two technology tracks in the morning. In the first track, Synopsys will unveil the next evolutionary step in the open-source Liberty® library format with Composite Current Source (CCS) modeling. The "CCS: An Industry Update" session will feature a new interoperability development that ensures broader industry involvement in CCS, plus technical advancements which address modeling challenges faced at process geometries of 90 nanometer (nm) and below. A parallel track, "Using EDA Databases: Milkyway™ and OpenAccess," will provide updates on these two open design databases. Presentations from designers and vendors will discuss using Milkyway and OpenAccess programming interfaces to build multi-vendor flows that allow for tighter design flow integration by enabling EDA tools to access design data directly.

The program will also feature a panel moderated by Steve Schulz, president and CEO of the Silicon Integration Initiative (Si2®). The panel, "Open Analog: The Final Frontier," will examine the progress, challenges and opportunities for creating open pcell descriptions and migration to an open environment for analog and custom designs based on OpenAccess.

The SPIRIT Consortium session will include John Goodenough, director of design technology at ARM, who will present updates that add reliability and stability to the proposed standard. Additionally, a major semiconductor company will present how they are using The SPIRIT Consortium's specification today in SoC development for 65 nm technology and Esterel Technologies will present how they are providing a clear path to implementation using The Consortium's specification to interface generated IP into coreAssembler.

Momentum for IEEE Std 1800™-2005 SystemVerilog continues to grow marked by widespread adoption of the language for both design and verification. The Forum's general session will feature the latest updates on the SystemVerilog standard from Dr. Karen Pieper, technical chair for the IEEE P1800 SystemVerilog Standard and an R&D director at Synopsys. The general session will continue with a presentation on "Organizing the Verification Solar System: SystemVerilog, VHDL, SystemC™ and OpenVera®." In this session, Synopsys Scientist Janick Bergeron will discuss how these languages interoperate and complement each other in advanced verification flows.

"The Synopsys EDA Interoperability Developers' Forum continues to be among the most important venues for the latest interoperability solution announcements and initiatives within the EDA industry," said Rich Goldman, vice president of Strategic Market Development at Synopsys. "This forum provides a unique opportunity for the EDA industry to exchange information and ideas about tool interoperability and efficient solutions for our customers' design flows."

About the EDA Interoperability Developers' Forum

For more information, to download presentations from previous forums, and to register for the 17th EDA Interoperability Developers' Forum, visit www.synopsys.com/devforum/may2006.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at www.synopsys.com.

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