Synopsys Offers First Certified TSMC 90-Nanometer USB 2.0 OTG PHY IP

DesignWare PHYs for Hi-Speed USB 2.0 and Hi-Speed USB OTG Developed with TSMC's Production-Proven 90-nm Libraries

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, and Taiwan Semiconductor Manufacturing Company (TSMC) today announced the availability of the Synopsys DesignWare® Hi-Speed Universal Serial Bus (USB) 2.0 intellectual property (IP) and Hi-Speed On-the-Go (OTG) physical layers (PHYs) for TSMC's Nexsys 90-nanometer (nm) process. This is the first production-ready PHY IP targeted at TSMC's 90-nm process to pass the official USB Hi-Speed OTG certification. Developed with TSMC's production-proven Nexsys standard cell libraries, the Synopsys DesignWare USB PHY IP provides a lower-risk path for embedded USB SoC designs. Thus, integrating the DesignWare PHY with system-on-chip (SoC) designs helps minimize area and power consumption while maximizing performance and yield.

"High-quality IP is a 'must have' for our customers," said Edward Wan, senior director of Design Service Marketing at TSMC. "As one of TSMC's IP partners, Synopsys is combining the TSMC process-optimized Nexsys library for advanced technologies with Synopsys' proven IP development methodology to deliver a high-quality, mixed-signal IP portfolio that meets our customers' needs."

The complete, certified DesignWare USB solution for designers targeting TSMC Nexsys process includes digital controllers and PHYs using the TSMC Nexsys library cells, and verification IP (VIP) for high-volume, cost-sensitive embedded USB 2.0 applications.

"Our complete USB solution, which includes USB controllers and VIP, gives designers a lower-risk, silicon-proven path to SoC design success," said Guri Stark, vice president of Marketing, Solutions Group at Synopsys, Inc. "The combination of high-speed DesignWare PHYs with the TSMC Nexsys process technology speeds time-to-results for high-yield USB 2.0 and OTG products and opens doors to high-volume applications in consumer and mobile market segments."

Availability

The DesignWare USB PHYs, digital cores and VIP are available from Synopsys today. The complete family of USB VIP is included in the DesignWare Library and VCS® Verification Library at no additional charge. The complete set of the TSMC libraries for 150-nm, 130-nm and 90-nm processes is available today at no additional cost to DesignWare Library licensees. The libraries can be downloaded from the Synopsys web: www.synopsys.com/designware.

About DesignWare Cores

Synopsys DesignWare Cores provide system designers with silicon-proven, digital and mixed-signal connectivity IP for some of the world's most recognized products, including communications processors, routers, switches, game consoles, digital cameras, computers and computer peripherals. Provided as synthesizable RTL source code or in GDSII format, these cores enable designers to create innovative, cost-effective systems-on-chips and embedded systems. Synopsys provides flexible licensing options for the DesignWare Cores. Each core can be licensed individually, on a fee-per-project basis or users can opt for the Volume Purchase Agreement, which enables them to license all the cores in one simple agreement. For more information on DesignWare IP, visit: www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at www.synopsys.com.

About TSMC

TSMC is the world's largest dedicated semiconductor foundry, providing the industry's leading process technology and the foundry industry's largest portfolio of process-proven library, IP, design tools and reference flows. The company operates two advanced twelve-inch wafer fabs, five eight-inch fabs and one six-inch wafer fab. TSMC also has substantial capacity

commitments at its wholly-owned subsidiary, WaferTech and TSMC (Shanghai), and its joint venture fab, SSMC. TSMC's corporate headquarters are in Hsinchu, Taiwan. For more information about TSMC please see www.tsmc.com.

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