Synopsys Releases Mixed-Signal PHY IP for SMIC 130-nm Process

High-Performance DesignWare IP for USB, PCIe, SATA and XAUI Now Available

PRNewswire-FirstCall
MOUNTAIN VIEW, Calif.

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that it has expanded its DesignWare® mixed-signal intellectual property (MSIP) portfolio with the release of connectivity IP for Semiconductor Manufacturing International Corporation's (SMIC's) 130-nanometer (nm) technology. The mixed-signal PHY IP supports the following protocols: USB, PCIe, SATA and XAUI. These PHYs are highly complex, process-tuned analog interfaces used in today's high-volume, highly integrated mobile terminals, home entertainment, computing, storage and networking applications. Additionally, high-performance DesignWare memory interface I/Os, such as DDR2 and mobile DDR, are available on SMIC's 130-nm process.

DesignWare mixed-signal PHY IPs are extremely differentiated compared to other PHY IP solutions in the market. They consume the lowest amount of power in the industry at least 30 percent lower than competitive solutions. This makes them ideal for mobile applications and saves on packaging costs. The PHY IP is also designed to have the lowest area, noise and jitter performance in the industry. It also features a uniquely robust architecture that makes it insensitive to process, voltage and temperature variations, helping ensure high yields. On-board diagnostics on the PCI Express, SATA and XAUI PHYs also enable inexpensive at-speed production testing that significantly reduces test-time budgets and costs.

"Synopsys has some of the highest performance and most differentiated mixed-signal IP on the market, and we are very pleased to announce our collaboration with them," said Paul Ouyang, vice president of Marketing at SMIC. "Together we can ensure that our customers have access to cost- effective, lowest power and lowest area USB 2.0 PHYs, Serdes-based PHYs for PCI Express, SATA and XAUI, and memory interface I/Os such as DDR2 and mobile DDR in our industry-leading 130-nm technology. With Synopsys, our customers can be assured of high-quality deliverables designed for low-risk system-on- chip (SoC) integration."

"We worked closely with SMIC to ensure that the low power and area of our PHYs and their high-yield characteristics are retained when manufactured in SMIC's 130-nm process," said Guri Stark, vice president of marketing for the Solutions Group at Synopsys. "We will continue collaborating with SMIC and aligning our mixed-signal IP roadmap with their technology roadmap to meet the demands of our mutual customers."

Availabilities

Synopsys DesignWare USB 2.0 nanoPHY IP, and DDR2 and mobile DDR memory interface I/Os are available now. PCI Express, SATA and XAUI PHYs are expected to be available in Q4 of calendar 2006.

About DesignWare Mixed-Signal IP

Synopsys enables designers to quickly integrate analog mixed-signal IP (MSIP) into next-generation SoCs with a comprehensive portfolio of high- performance PHYs for the PCI Express, SATA, XAUI, and USB protocols. In addition, the MSIP offering also includes a complete suite of I/O libraries and high-performance integrated memory PHYs. Available for industry-leading processes, DesignWare MSIP meets the needs of today's high-speed designs for the networking, storage, computing and consumer electronics markets. The DesignWare MSIP offering is complemented by a comprehensive suite of digital controller cores and verification IP to provide chip developers with a complete solution for SoC integration. Each MSIP can be licensed individually on a fee-per-project basis, or customers can opt for the Volume Purchase Agreement, which enables them to license all the MSIP in one simple agreement.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

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