

Synopsys IP for PCI Express 2.0 (Gen II) Passes PCI-SIG Compliance

First IP Provider to Pass PCI-SIG Compliance Testing With Complete PHY and Digital Controller Solution

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that its DesignWare® PHY and digital controller intellectual property (IP) for PCI Express™ 2.0 (Gen II) is the first complete Gen II IP solution from a single vendor to pass the latest compliance testing at the PCI-Special Interest Group (PCI-SIG) workshop. Compliance helps ensure interoperability while minimizing risk and reducing time to market for designers using complex, high-performance PCI Express interfaces. Designers depend on the market-leading DesignWare PHY, digital cores and verification IP to provide a complete, silicon-proven solution for incorporating PCI Express connectivity into system-on-chip (SoC) designs.

The DesignWare digital controller IP for PCI Express 2.0 is fully compliant with the recently released PCI Express 2.0 specification and has successfully passed the latest PCI Express compliance testing at the PCI-SIG interoperability workshop held in the United States in December 2006. The DesignWare digital controllers for PCI Express 2.0 support the 2.5 and new 5.0 gigabits per second data rates of the PCI Express 2.0 specification and provide a complete portfolio of IP for the design of Endpoint, Root Complex, Switch and Bridge applications. Designers of SoCs using AMBA® 3 AXI™ and AMBA AHB™ on-chip interconnect can easily add PCI Express 2.0 functionality to their designs by using the DesignWare Bridge for PCI Express to AMBA 3 AXI or DesignWare Bridge for PCI Express to AMBA AHB IP.

"Designers expect Synopsys, as the leader in PCI Express IP, to aggressively implement the industry's PCI Express roadmap and to test our IP at compliance workshops as early as possible," said John Koeter, senior director of marketing, Synopsys Solutions Group. "We have been providing PCI Express 2.0 support to our customers since the 0.3 version of the Gen II specification. This has not only allowed our customers' design teams to begin early Gen II development, but has also enabled the DesignWare® PHY for PCI Express and digital controller (IP) for PCI Express 2.0 to pass the latest compliance tests on the first attempt."

At the December 2006 PCI-SIG v1.1 compliance workshop, Synopsys also tested DesignWare PHY IP, implemented in multiple foundry process nodes from TSMC and SMIC. The DesignWare PHY IP is fully compliant with the PCI Express specification and the PIPE interface standard. It offers superior performance, area, power and testability. DesignWare PHYs substantially exceed the PCI Express electrical specifications in such key performance areas as jitter margin and receive sensitivity while containing advanced on-die diagnostics, including an on-die oscilloscope.

The DesignWare Verification IP (VIP) Suite for PCI Express supports the directed and random methodologies defined in the Verification Methodology Manual (VMM) for SystemVerilog. The DesignWare VIP Suite for PCI Express is available as a standalone product, as well as being included in the DesignWare Library and VCS Verification Library. The DesignWare VIP is also included with the DesignWare digital controller for PCI Express 2.0, enabling designers to test the integration of the DesignWare digital controller IP in their SoC designs.

PCI-SIG released the PCI Express Base 2.0 specification in January, 2007. Synopsys' DesignWare digital controller IP for PCI Express for 2.0 conforms to this specification and is included in the PCI-SIG Integrators List, having demonstrated compliance to the version 1.1 specification, the most advanced compliance workshop offered by the PCI-SIG.

Availability

The DesignWare digital controller (Endpoint, Root Complex, Dual Mode, Switch and Bridge) for PCI Express 2.0 is available now. The DesignWare PHY IP for PCI Express is available today in lane widths from x1 to x16 and in multiple process nodes from leading foundries including: TSMC, SMIC, IBM, and Chartered. The DesignWare VIP Suite for PCI Express is available now.

About DesignWare Cores

Synopsys DesignWare Cores provide system designers with silicon-proven, digital, and mixed-signal connectivity IP for some of the world's most recognized products, including communications processors, routers, switches, game consoles, digital cameras, computers and computer peripherals. Provided as synthesizable RTL source code or in GDS format, these cores enable designers to create innovative, cost-effective system-on-chips and embedded systems. Synopsys provides flexible licensing options for the DesignWare Cores. Each core can be licensed individually, on a fee-per-project basis, or users can opt for the Volume Purchase Agreement, which enables them to license all the cores as part of one simple agreement. For more information on DesignWare IP, visit: <http://www.designware.com/>.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at <https://www.synopsys.com/> .

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Editorial Contacts:
Yvette Huygen
Synopsys, Inc.
650-584-4547
yvetteh@synopsys.com

Ellen Van Etten
MCA
970-778-6094
evanetten@mcapr.com

SOURCE: Synopsys, Inc.

CONTACT: media, Yvette Huygen of Synopsys, Inc., +1-650-584-4547, or yvetteh@synopsys.com; or media, Ellen Van Etten of MCA, +1-970-778-6094, or evanetten@mcapr.com, for Synopsys, Inc.

Web site: <https://www.synopsys.com/>
