

Synopsys Donates Technology for Low Power Design to Accellera Standards Organization

Technology Proven to Help Customers Achieve Ultra Low Power IC Designs

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that it has donated power management technology to Accellera, the Electronic Design Automation (EDA) organization focused on electronic design automation standards. The donation includes power management commands, SystemVerilog constructs, VHDL constructs, and the Switching Activity Interchange Format (SAIF), all in support of Accellera's Unified Power Format technical subcommittee's efforts. Under the Unified Power Format activities, the design community, EDA tool suppliers and standards bodies are working together to produce an open and inclusive standard for low power design by January 2007.

"The donation by Synopsys to the Unified Power Format technical subcommittee is much appreciated and complements donations from other Accellera members," said Shrenik Mehta, Accellera chair. "We look forward to delivering a standard based on industry-wide contributions that will quickly meet the demands of end-customers."

Synopsys is an industry leader in providing solutions for low power design automation. Its low power solutions have been proven through multiple successful advanced low power tapeouts to enable customers to develop more competitive products. The Synopsys Galaxy™ and Discovery™ platform solutions for low power design span RTL synthesis, physical implementation, verification, and analysis. This allows simulation of power-down blocks, equivalency- and design-checking of advanced low power designs, inference of consistent constraints as early as possible, and communication of the designer's power intent throughout the entire design and verification flow.

"Many customers worldwide utilize Synopsys' low power technology to produce their most advanced low power designs," said Rich Goldman, vice president of Strategic Market Development at Synopsys, Inc. "By contributing our technology to the Accellera Unified Power Format technical subcommittee, Synopsys demonstrates its dedication to allow all designers and EDA suppliers to utilize its proven technology as a comprehensive standard for low power design."

About Unified Power Format

The Unified Power Format technical subcommittee was formed by active participation from design community, EDA suppliers and standards bodies. The charter of the technical subcommittee is to deliver industry wide standard for low power design. The Unified Power Format technical subcommittee is open to everyone without requiring NDAs or proprietary licenses. It's inclusive: All are invited to participate in the Unified Power Format technical subcommittee and donate technology to the standard. It's fast: The standard expected to be available by January 2007.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at <http://www.synopsys.com>.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of the safe harbor provisions of Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected date of availability of the Unified Power Format. These statements are based on Synopsys' current expectations and beliefs. The actual date of release of the format could be different as a result unforeseen difficulties encountered completing the definition, specification and implementation of the format, uncertainties attendant to any new technology offering and certain statements contained in the section of Synopsys' Quarterly Report on Form 10-Q for the fiscal quarter ended July 31, 2006 entitled "Factors That May Affect Future Results."

NOTE: Synopsys is a registered trademark of Synopsys, Inc. Galaxy and Discovery are trademarks of Synopsys. Any other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

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