New SystemVerilog Book Helps Engineers Master the Adoption of the VMM Methodology

VhdlCohen Publishes A Pragmatic Approach to VMM Adoption: 'A SystemVerilog Framework for Testbenches'

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VhdlCohen Publishing, a verification service provider, today announced the immediate availability of a new book, "A Pragmatic Approach to VMM Adoption: A SystemVerilog Framework for Testbenches," a companion book to the Verification Methodology Manual (VMM) for SystemVerilog. The new book is co-authored by Ben Cohen, a well-known consultant and author of several technical books addressing the effective use of Verilog and VHDL for logic design and verification; Srinivasan Venkataramanan, verification solutions applications manager at Synopsys, Inc.; and Ajeetha Kumari from Contemporary Verification Consultants Pvt. Ltd., of Bangalore, India. The book is intended for engineers involved in the increasingly important task of verifying the functionality of complex digital electronic circuits. It provides background on the coverage- driven, constrained-random verification environments detailed in the VMM book and offers advice on adoption and deployment. The book presents by example the practical application of the VMM methodology using SystemVerilog.

"Our experience with the VMM methodology has been very positive because it requires a minimal knowledge of object-oriented programming to put the verification effort where it belongs -- into the problem at hand," said Ben Cohen, co-author of "A Pragmatic Approach to VMM Adoption, VhdlCohen Publishing." "It also brings a common look and feel to every VMM-based verification environment and provides a mature framework that has endured years of active use."

"A Pragmatic Approach to Adopting VMM" is intended to help design and verification engineers come up to speed in the design of SystemVerilog transaction-based testbenches that comply with the VMM for SystemVerilog. With complete, compilable and executable examples, it will help users adopt the VMM methodology in the creation of comprehensive constrained-random and directed verification environments using a transaction-level modeling approach. All code examples are available for download. The book makes use of the most practical rules of the VMM methodology to demonstrate and show how to create a VMM-compliant testbench.

"One of the reasons that we decided to write 'A Pragmatic Approach to Adopting VMM' is because we truly believe that the VMM methodology is a framework that allows you to quickly create fast, reusable, and extendable testbenches using SystemVerilog," continued Cohen. "This book adds some additional explanations and practical, complete examples to emphasize the features of the VMM methodology. This book also presents the results of real- life experiences applying the methodology to various problems, providing useful insight and enabling faster SystemVerilog testbench adoption."

The book demonstrates features and techniques that support transactions, generators, command transactors (such as bus functional models), logging of messages, and the verification environment. Since SystemVerilog includes object-oriented programming (OOP) capabilities, the book provides applications of OOP design patterns such as factories and callbacks. In addition, it addresses advanced topics that relate to different applications and verification, including the synchronization of events through the notification services, channel broadcast, channel scheduling, and the role of coverage.

"The advanced techniques detailed in the VMM for SystemVerilog deliver tremendous value in terms of verification productivity and predictability, but some training is helpful at making adoption as quick and easy as possible," said Janick Bergeron, Synopsys Scientist. "I am pleased to welcome 'A Pragmatic Approach to Adopting VMM' to the canon of VMM-related literature. I hope users will find it helpful in appreciating the power of the VMM methodology and ease their adoption of it."

"'A Pragmatic Approach to Adopting VMM' can be seen as a practical review of best practices for writing SystemVerilog-based testbenches," said Alain Raynaud, Technical Director, EVE USA, Inc. "Companies should adopt the VMM methodology, if only to save cost, as verification engineers have better things to do than redevelop and learn a new testbench environment every time they change projects."

"A Pragmatic Approach to VMM Adoption: A SystemVerilog Framework for Testbenches" is available now from VhdlCohen Publishing for $125 US. To find out more about the book or to order it online, please visit: http://www.systemverilog.us/vmm_info.html .

About VhdlCohen Publishing

VhdlCohen Publishing provides verification education and services and has teamed with Stuart Sutherland of Sutherland HDL, Inc., and a member of the IEEE P1800 SystemVerilog Working Group, to provide training of several verification courses including the application of VMM and SystemVerilog assertions. VhdlCohen was founded in 2000 in Palos Verdes Peninsula,

California. More information can be found at www.systemverilog.us .

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