Synopsys DFT MAX Cuts Test Costs 90 Percent in Actions Semiconductor Designs

DFT MAX Reduces Test Data Volume and Test Application Time for High-Quality Testing

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that Actions Semiconductor Co., Ltd has adopted the Synopsys DFT MAX scan compression automation solution for its 0.13-micron systems-on-chip (SoC) designs, resulting in a 90-percent reduction in tester-related costs. DFT MAX implements scan data compression on-chip to significantly reduce the amount of test time and test data required to execute high-quality manufacturing tests.

"As the leading supplier of portable multimedia player SoCs, Actions' products are designed into a vast range of portable consumer electronics worldwide. Our design team needed a proven compression solution that was easy to use and could decrease the costs of testing our next-generation PMP SoCs," said Shawn Lee, chief technology officer of Actions Semiconductor. "We quickly got DFT MAX working on a multi-million-gate design thanks to its tight integration in the Synopsys Galaxy™ Design Platform. DFT MAX achieved more than 90 percent compression with an overhead of less than 500 extra gates. For these reasons, Actions has adopted DFT MAX for our future SoC designs."

Standard stuck-at test patterns are ineffective detecting many timing-sensitive defects, so semiconductor companies are now using transition delay tests to cover these defects at 0.13-micron geometries and below. Applying both types of tests has led to an explosion in the total number of test patterns required to properly test a device, even as design complexity has increased. The resulting inflation in both pattern count and test data volume per pattern has increased the time required to test each device, creating bottlenecks in production testing. DFT MAX automatically implements compression on-chip to substantially reduce test data volume and test application time while minimizing the impact on silicon area.

"Actions' decision to use DFT MAX to help meet its quality and cost goals is testimony to the effectiveness of Synopsys' Galaxy test solutions," said Graham Etchells, director of Test Marketing, Synopsys Implementation Group. "Semiconductor companies like Actions require a fast path to lowering the costs of testing nanometer designs, and DFT MAX is the compression solution they are adopting to significantly reduce test data volume, application time and cost without impacting downstream physical design flows."

Using DFT MAX requires no expertise in test compression techniques. Its gates-only adaptive scan architecture is the most area-efficient solution available. By avoiding the use of complex sequential state machines for compression/decompression, the adaptive scan architecture disperses test logic throughout the design, alleviating wire-routing congestion and reducing silicon area overhead cost. Working seamlessly within Synopsys' Galaxy Design Platform, DFT MAX produces predictable results with little to no impact on timing.

About Actions

Actions Semiconductor is one of China's leading fabless semiconductor companies that provides mixed-signal and multimedia SoC solutions for portable consumer electronics. Actions Semiconductor products include SoCs, firmware, software, solution development kits, as well as detailed specifications of other required components and the providers of those components. Actions Semiconductor also provides total product and technology solutions that allow customers to quickly introduce new portable consumer electronics to the mass market in a cost effective way. The company is headquartered in Zhuhai, China, with offices in Beijing and Shenzhen. For more information, please visit the Actions Semiconductor website at http://www.actions-semi.com/ .

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at www.synopsys.com .

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CONTACT: media, Sheryl Gulizia of Synopsys, Inc., +1-650-584-8635, or sgulizia@synopsys.com; or media, Rachel Modena Barasch of MCA, Inc., +1-650-325-7547, or rbarasch@mcapr.com, for Synopsys, Inc.

Web site: http://www.actions-semi.com/
https://www.synopsys.com/