Synopsys Showcases Galaxy 2004 Unified Design-for-Test Solution at International Test Conference

Top Customers Present Latest Success With Synopsys Test Solution at 12th Annual SIG Event

Synopsys, Inc. (NASDAQ: SNPS), the world leader in semiconductor design software, today announced that it will showcase its complete Galaxy™ 2004 unified design-for-test solution at the International Test Conference (ITC) from Tuesday, October 26 through Thursday, October 28. The Galaxy 2004 test solution delivers a comprehensive test automation solution that offers integrated circuit designers rapid test implementation, high quality manufacturing test diagnostics and working silicon with low test cost. Synopsys also has announced that it will host its 12th annual Special Interest Group (SIG) event at ITC, a customer event where Synopsys customers speak on the industry's advancements in test and have a chance to meet and mingle with Synopsys' world-class test experts.

"The Synopsys Galaxy 2004 test automation solution offers a comprehensive family of products for mainstream to high-performance semiconductor designs. It incorporates capabilities that enable designers to achieve rapid design-for-test (DFT) closure and sign off on the testability of their mainstream chips, as well as reduce test cost and time and data volume for their most complex designs," said Antun Domic, senior vice president and general manager, Implementation Group. "ITC is an important venue to demonstrate the significance of this solution, and it allows Synopsys to reach out to product designers and test engineers responsible for IC test."

Synopsys' SIG Event

Synopsys will hold its annual SIG event at ITC, hosted by Antun Domic, senior vice president and general manager, Implementation Group, with presentations by top customers. SIG will be held on Monday, October 25 at the Levine Museum in Charlotte, North Carolina from 5:30 p.m. to 8:30 p.m. SIG offers a casual setting to meet and mingle with world-class test experts, including Thomas Williams (Synopsys and IEEE Fellow), John Waicukauski (Synopsys Fellow), Rohit Kapur (Synopsys Scientist, IEEE Fellow, and author of CTL for Test Information of Digital ICs) and Denis Martin (Synopsys Scientist). Synopsys customers may register at: https://www.synopsys.com/cgi-bin/itc04/sigreg1.cgi .

Synopsys at ITC

ITC will be held from Tuesday, October 26 through Thursday, October 28 at the Charlotte Convention Center in North Carolina. Synopsys will be showcasing Galaxy Test at booth #1211. Synopsys will be demonstrating its unified design and test solution for layout-driven DFT synthesis -- the fastest path to DFT closure, and will highlight its industry-leading physical failure analysis solution for deep sub-micron test using Credence EmiScope® -- accelerating test analysis from days to hours.

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at https://www.synopsys.com/.

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