Synopsys and Virage Logic Collaborate on Test Reference Design Flow to Deliver Embedded Memory Test

Comprehensive Test Flow Links Galaxy Platform With STAR Memory System

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, and Virage Logic Corporation (NASDAQ: VIRL), a pioneer in Silicon Aware IP™ and a leading provider of semiconductor intellectual property (IP) platforms, today announced initial availability of a test reference design flow for cost-effective testing and repair of embedded memories for system-on-chip (SoC) designs. The validated test design flow for 90-nanometer (nm) and 65-nm processes is based on the Synopsys Galaxy™ test platform and Virage Logic's Self-Test and Repair (STAR) Memory System™. The reference design flow provides designers an automated and comprehensive solution to address time-to-market pressures and challenges of creating high-quality manufacturing tests for complex designs that contain multiple embedded memories. The collaboration will continue with a second validated Galaxy test reference flow, which will integrate the testing of Synopsys DesignWare® IP memories within Virage Logic's STAR Memory System.

"This latest collaboration with Synopsys further validates Virage Logic's commitment to providing customers with integrated design flows that help accelerate their silicon success, particularly as they move to the more advanced process nodes of 90nm and 65nm," said Jim Ensell, senior vice president of marketing and business development at Virage Logic. "With STAR Memory System customers achieving yield improvements of up to 250 percent, we're confident the new Synopsys-Virage Logic reference design flow will enable our mutual customers to meet their SoC test, yield, and time-to-market goals."

"Today's consumer products often contain dozens if not hundreds of memories and register files," said Bijan Kiani, vice president of marketing, Synopsys Implementation Group. "Creating high-quality manufacturing tests that deliver good coverage for the design logic as well as the memory content is a challenging and time-consuming task. The Synopsys-Virage Logic collaboration will help designers address these challenges by ensuring interoperability between Virage Logic's STAR Memory System RTL flows and the test synthesis flows within Synopsys' Galaxy test platform. Synopsys customers using DFT MAX physical-aware scan compression to reduce test costs and increase test quality will now benefit from a verified, automated flow that includes comprehensive testing of embedded memories."

Customer Support

A reference design and detailed application note describing the test reference flow will be available this quarter on Synopsys' SolvNet online support site at http://solvnet.synopsys.com/ . The STAR Memory System and supporting products are currently available from Virage Logic. Customers may request information by contacting Virage Logic at info@viragelogic.com.

About Synopsys Galaxy Test Platform

The Synopsys Galaxy test platform is an advanced design-for-test (DFT) solution that has been consistently proven in silicon to predictably achieve the highest test quality while significantly reducing the costs of test. This award-winning platform includes the TetraMAX® automatic test pattern generator (ATPG), one of the industry's most advanced pattern generation solutions for targeting and diagnosing nanometer defects, and DFT MAX physical-aware adaptive scan compression, the industry's lowest area-overhead solution used to significantly reduce tester costs. These products work together within the Galaxy Design Platform to help eliminate costly and time- consuming design iterations between front-end and back-end flows, and achieve rapid DFT closure and sign-off for even the most complex SoCs.

About Virage Logic's STAR Memory System

The STAR Memory System provides the most integrated solution for the cost- effective embedding, on-chip testing, and repairing of multi-megabit memories. High-speed, high-density and ultra-low-power STAR and Area, Speed and Power (ASAP) Memory™ memories can be incorporated into a STAR Memory System to address a broad range of SoC design requirements. The STAR Memory System consists of a complete solution allowing users to select and automatically integrate all of the pieces associated with the system. The STAR Shared Fuse Processor allows users to reduce routing complexity and drastically reduce fuse area while the STAR Builder automated integration tool enables users to better meet aggressive time-to-market requirements. With customers experiencing yield improvements of up to 250 percent, the STAR Memory System can potentially save millions of dollars in recovered silicon, substantially reduce test costs, and achieve shorter time-to-volume.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at www.synopsys.com .

About Virage Logic Corporation

Founded in 1996, Virage Logic Corporation rapidly established itself as a technology and market leader in providing advanced embedded memory intellectual property (IP) for the design of complex integrated circuits. Now, as the company celebrates its 10th anniversary, it is a global leader in semiconductor IP platforms comprising embedded memories, logic, and I/Os and is pioneering the development of a new class of IP called Silicon Aware IP™. Silicon Aware IP tightly integrates Physical IP (memory, logic and I/Os) with the embedded test, diagnostic, and repair capabilities of Infrastructure IP to help ensure manufacturability and optimized yield at the advanced process nodes. Virage Logic's highly differentiated product portfolio provides higher performance, lower power, higher density and optimal yield to foundries, integrated device manufacturers (IDMs) and fabless customers who develop products for the consumer, communications and networking, hand-held and portable, and computer and graphics markets. The company uses its FirstPass-Silicon™ Characterization Lab for certain products to help ensure high quality, reliable IP across a wide range of foundries and process technologies. The company also prides itself on providing superior customer support and was recently named Customer Service Leader of the Year in the Semiconductor IP Market by Frost & Sullivan. Headquartered in Fremont, California, Virage Logic has R&D, sales and support offices worldwide. For more information, visit www.viragelogic.com .

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including Synopsys' and Virage Logic's expectations of the future features and benefits of their collaboration on reference design flows to provide embedded memory test and repair capabilities for system-on- chip designs. These statements are based on Synopsys' and Virage Logic's current expectations and beliefs. Actual results could differ materially from these statements as a result of difficulties implementing the test and repair capabilities for a particular customer's design or an IC manufacturer's process, uncertainties attendant to any new semiconductor design reference flow and certain statements contained in Synopsys' Quarterly Report on Form 10-Q for the fiscal quarter ended July 31, 2006 and in Virage Logic's Annual Report on Form 10-K for the period ended September 30, 2005.

NOTE: Synopsys, DesignWare, and TetraMAX are registered trademarks of Synopsys, Inc. Galaxy is a trademark of Synopsys, Inc. Any other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

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