Mentor Graphics and Synopsys Offer SystemVerilog Seminars for Users of the Verisity e Language

Industry Leaders to Demonstrate Immediate Benefits of Using SystemVerilog for Advanced Verification

PRNewswire- FirstCall
MOUNTAIN VIEW, Calif., and WILSONVILLE, Ore.

Two leaders in advanced verification solutions -- Mentor Graphics (NASDAQ: MENT) and Synopsys (NASDAQ: SNPS) -- are presenting a series of free "eScape to SystemVerilog" technical seminars that provide guidance to users of Verisity's e language to transition to a standards-based verification methodology built on SystemVerilog. The first set of seminars in this worldwide series will take place in San Jose on March 2, 2005. Subsequent seminars will take place in Dallas and Boston, with additional locations in North America, Europe, Israel, Japan, Korea, India and Taiwan to be added at a later date.

The "eScape to SystemVerilog" technical seminars will provide practical demonstrations on how users of Verisity's e language can apply SystemVerilog to speed verification and find more bugs, faster. Attendees will learn about SystemVerilog's verification capabilities and gain insight on leveraging these capabilities to increase productivity and design quality. Extensive practical examples will be used to illustrate the verification concepts and methods presented.

"SystemVerilog delivers tremendous benefits for the electronics industry," said Manoj Gandhi, senior vice president and general manager, Verification Group at Synopsys. "Synopsys pioneered the SystemVerilog standardization effort with multiple technology donations and continues to lead with broad support in our design and verification tools. SystemVerilog's unified design and verification capabilities help enable customers to achieve significant productivity gains as compared to point-tool solutions."

"The interest in SystemVerilog is very strong," said Robert Hum, vice president and general manager, Design Verification and Test Division at Mentor Graphics. "Many companies and organizations that have led the evolution in verification by using proprietary languages such as e are transitioning to a standards-based verification methodology built on SystemVerilog. Mentor Graphics has always taken the lead on supporting standards and continues to do so with its Scalable Verification™ solution based on SystemVerilog."

Experts in verification methodology and SystemVerilog language features will present the "eScape to SystemVerilog" seminars in an engineering, application-focused fashion. Topics to be covered include language basics, constrained-random test generation, abstraction and reuse, functional coverage, inter-process communication, assertions and verification environment structure.

Seminar Schedule and Locations

The "eScape to SystemVerilog" technical seminar dates and locations in the United States are:

March 2, 2005 - San Jose, California
March 3, 2005 - Dallas, Texas
March 4, 2005 - Boston, Massachusetts

Additional locations will be announced soon. For more details on currently scheduled locations and to register, please visit http://www.systemverilognow.com/.

About SystemVerilog

SystemVerilog, the first hardware description and verification language (HDVL), is an extension to the IEEE Std 1364™-2001 Verilog HDL and offers advanced design features to tackle the most complex next-generation designs, provides comprehensive testbench and assertions capabilities for integrated high-performance verification and offers a designer-friendly direct programming interface for efficient interaction with C/C++ models, code and algorithms. For more information about SystemVerilog, visit https://www.synopsys.com/verification.html .

About Mentor Graphics

Mentor Graphics Corporation is a world leader in electronic hardware and software design solutions, providing products, consulting services and award-winning support for the world's most successful electronics and semiconductor companies. Established in 1981, the company reported revenues over the last 12 months of over $700 million and employs approximately 3,850 people worldwide. Corporate headquarters are located at 8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777;

Silicon Valley headquarters are located at 1001 Ridder Park Drive, San Jose, California 95131-2314. World Wide Web site: https://www.mentor.com/ .

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

SOURCE: Synopsys, Inc.

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Web site: http://www.systemverilog.org/

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