Semiconductor Firms Collaborate With Synopsys to Validate New ATPG Technology

Significant Improvement in the Quality of At-Speed Testing Expected from Test Pattern Generation Based on Precise Timing

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that it has collaborated with several semiconductor firms to test a new automatic test pattern generation (ATPG) technology designed to increase the quality of manufacturing tests by targeting small delay defects. The enhanced capability uses precise timing information from the Synopsys PrimeTime® sign-off static timing analysis tool to test for small circuit delays that could result in timing failures when parts are run at-speed. Because traditional transition-delay ATPG does not directly target small delay defects, the new approach can further improve quality and reduce test escapes for digital integrated circuits (ICs) sensitive to small delay defects. Synopsys will demonstrate the new technology at this year's International Test Conference (ITC) in Santa Clara, Calif., October 24-26 (booth #112).

The Semiconductor Technology Academic Research Center (STARC), a research and development consortium founded by major Japanese semiconductor companies, has been working with Synopsys for the past two years to help develop and validate the technology. "STARC considers small delay defects a critical quality issue for our member companies as they design more circuits at 90- nanometer technologies," said Takashi Aikyo, senior manager of the Test and Diagnosis Group at STARC. "We appreciate the early interest from Synopsys, and we now look forward to working with our member companies and Synopsys to deploy this new test technology on production designs."

"Subtle process variations at 90nm and below can introduce small delays that adversely affect the most timing-sensitive paths in a design," said Graham Etchells, director of test marketing, Synopsys Implementation Group. "These small delay defects can remain untested using traditional transition- delay ATPG because it lacks the precise timing information required to explicitly target them. The new technology uses precise timing data from PrimeTime sign-off analysis to test small delay defects. We expect this innovation will result in a significant improvement in the quality of at-speed testing, leading to fewer test escapes and lower test cost."

Highly-accurate timing analysis is the key to testing small delay defects. Designers can pass parasitic information from Synopsys' Star-RCXT™ sign-off extraction tool to the PrimeTime tool for static timing analysis, then use pin-slack information generated from the timing analysis to create small- delay-defect ATPG patterns. Reports and histograms provide metrics for measuring the test quality of a design in the presence of small delay defects. The new ATPG technology is consistent with existing design for test (DFT) methodologies and does not require changes to a design.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including Synopsys' expectations of the benefits of the new ATPG technology being demonstrated by Synopsys. These statements are based on current expectations and beliefs. Actual results could differ materially from these statements as a result of development issues encountered while adapting the ATPG technology for commercial release and use, uncertainties attendant to any new technology and certain statements contained in the section of Synopsys' Quarterly Report on Form 10-Q for the fiscal quarter ended July 31, 2006 entitled "Management's Discussion and Analysis of Financial Condition and Results of Operations - Factors That May Affect Future Results."

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