Synopsys Donation of Variation-Aware Extension to SPEF Format Approved by IEEE 1481 Working Group

SPEF Extension Provides Consistent and Accurate Representation of Parasitic Sensitivity Information at 65 Nanometers and Beyond

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that the IEEE 1481 working group has approved its proposal for an extension to the Standard Parasitic Exchange Format (SPEF) for process and temperature variation. This proposal enhances the existing IEEE standard 1481-1999 for SPEF by providing a common medium to pass sensitivity-based parasitic information between electronic design automation (EDA) tools. The Synopsys proposal includes key extensions that accurately and concisely represent interconnect parasitic sensitivity information required for sub-65-nanometer (nm) processes. The draft standard for the SPEF extension is now pending balloting and approval by the IEEE Standards Board.

With shrinking device technologies, accurate modeling of random process variation for interconnects has become a requirement. Extraction and analysis tools use statistical techniques to model these effects. However, efficient and accurate statistical analysis requires sensitivity of interconnect parasitics with respect to physical and electrical process parameters. A standard sensitivity-based SPEF format would enable parasitic extraction tools to create a netlist with nominal values of parasitics and their sensitivities to interconnect process parameters, which can then be easily read by analysis, simulation and implementation tools.

"An industry-standard SPEF format with the sensitivity extension is invaluable for our leading-edge designs at 65nm," said Adrian Hartog, senior vice president at AMD. "A common standard will allow us to seamlessly leverage various EDA tools that support the new format in our statistical design flow. We applaud Synopsys' proposal to advance interoperability in the industry and look forward to its adoption as an industry-wide standard."

"The SPEF extension is critical to address the emerging process- and temperature-variation challenges for sub-65nm designs, as emphasized by the support from industry-leading semiconductor companies such as AMD," said Rich Goldman, vice president, Strategic Market Development at Synopsys. "By proactively working with the IEEE 1481 Working Group and driving a single sensitivity-based SPEF standard, Synopsys has demonstrated its commitment to further openness and interoperability in the electronics industry."

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

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