NetSilicon Cuts Verification Time and Effort in Half With Synopsys' Vera Tool

Powerful Testbench Automation in Synopsys Discovery™ Verification Platform Enables NetSilicon to Achieve First-Silicon Success

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that NetSilicon, Inc., a Digi International® Company (NASDAQ: DGII), achieved first-silicon success using Synopsys' Vera® testbench automation tool and the VCS® comprehensive RTL verification solution as the backbone of its NS9750 NET+ARM processor verification environment. The powerful combination of Synopsys' verification solutions in the Discovery™ Verification Platform enabled NetSilicon to cut verification time in half and meet an aggressive schedule for delivering samples to initial customers.

"After evaluating available testbench solutions on the market, we selected the Synopsys Vera tool because of its superior capabilities for constrained-random stimulus generation, ease of adoption and evolutionary path to VCS Native Testbench technology," said Brad Hollister, verification lead at NetSilicon. "Even though this chip was more complex than our previous projects, it was functionally correct on first silicon. Doing this project without the Vera tool would have likely required at least twice the number of people and twice the elapsed time."

"NetSilicon's experience clearly demonstrates the benefits of using the industry's most advanced verification solutions," said Farhad Hayat, vice president of Marketing, Verification Group, Synopsys, Inc. "The powerful combination of the Vera tool's advanced testbench automation and the VCS solution's high performance and built-in bug-finding technologies helps our customers verify their most challenging chips on time and on budget."

About the Latest Release of the Vera Tool

The Vera 6.3 version adds numerous productivity enhancements that make it easier to set up a coverage-driven verification environment and debug the results of running constrained-random tests. These enhancements include a new debugger, a VHDL template generator, the Vera tool-to-SystemC™ transaction level interface, and several new language features. The tool includes the production release of a completely new, robust, high-performance testbench debugger with a faster GUI and added capabilities. It also now has an automated procedure for interface generation, making the connection of VHDL designs to Vera testbenches easier. In addition to pin-level support for SystemC models, version 6.3 adds the capability to pass transaction objects between the Vera tool and SystemC models to facilitate a single testbench for transaction-level and RTL models.

Synopsys Discovery Verification Platform

The Discovery Verification Platform is a unified environment that provides high performance and efficiency of interaction among all platform components, including mixed-HDL simulation, mixed-signal, system-level verification, assertions, verification intellectual property, code coverage, functional coverage, testbenches and formal analysis. Combined with support for industry-standard hardware design and verification languages, including Verilog, VHDL, SystemVerilog, SystemC and OpenVera®, and Synopsys' proven RVM, the Discovery Verification Platform helps designers achieve higher levels of verification productivity by contributing to first-time silicon success within required project cycles.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at https://www.synopsys.com/ .

NOTE: Synopsys, OpenVera, VCS and Vera are registered trademarks of Synopsys, Inc. Discovery is a trademark of Synopsys, Inc. All other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

SOURCE: Synopsys, Inc.

CONTACT: Isela Warner of Synopsys, Inc., +1-650-584-1644, or igamboa@synopsys.com; or Sarah Seifert of Edelman, +1-650-968-4033, or sarah.seifert@edelman.com, for Synopsys

Web site: https://www.synopsys.com/