# Synopsys to Distribute TSMC'S Libraries Through DesignWare Library

Distribution Agreement Builds on Previous RTL-to-GDSII Design Flow Collaboration

Synopsys, Inc. (NASDAQ: SNPS), the world leader in semiconductor design software, and Taiwan Semiconductor Manufacturing Company (TSMC) (NYSE: TSM), the world's largest semiconductor foundry, announced today TSMC's libraries will now be distributed through Synopsys' DesignWare® Library. This collaboration provides the more than 25,000 DesignWare Library users, at no additional cost, access to standard cell and I/O libraries created by TSMC and optimized for the company's 0.15-, 0.13-micron and 90 nanometer (nm) Nexsys(SM) Technology for SoC foundry processes. Synopsys will also offer TSMC's memory libraries for an additional fee. The combination of libraries, proven methodology and industry-leading intellectual property (IP) technical support will help reduce design risk and accelerate time-to-volume for designers.

This agreement is the latest collaboration in a long-term relationship between the two companies. The agreement provides that both companies will optimize TSMC's standard cell and I/O libraries and produce design flows that deliver higher productivity and design quality to users. The libraries are validated in TSMC Reference Flow 4.0, an RTL-to-GDSII flow comprised of leading EDA tools, including tools from the Synopsys Galaxy™ platform. As a result of cooperative research and development efforts, TSMC libraries currently support all Synopsys views used in the design flow, including: .lib, with noise modeling capabilities; .db; .plib; .pdb; Apollo™; Astro™; and the Synopsys Milkyway™ design database, as well as other EDA formats. This integration was achieved using Synopsys' Liberty™ open standard library specification and Milkyway.

TSMC libraries are developed and process-tuned to TSMC semiconductor technologies. Each logic and I/O cell is validated in silicon and meets the company's rigorous library quality criteria. TSMC libraries are in volume production, in multiple customer designs.

"During the past three years, we've worked closely with Synopsys to enhance TSMC's libraries for optimal performance and operation in TSMC Reference Flows, which include tools from Synopsys' Galaxy Design Platform," said Genda Hu, vice president of marketing at TSMC. "Offering TSMC's libraries through Synopsys' DesignWare Library provides easy access for a broad population of designers targeting TSMC's advanced technologies."

"Synopsys and TSMC are responding to designer requests to provide a complete RTL-to-GDSII design environment," said John Chilton, senior vice president and general manager of Synopsys' Solutions Group. "By adding to Synopsys' already extensive DesignWare IP Solution, this new library distribution agreement extends our collaborative efforts to decrease designers' project risk and time-to-production on TSMC's deep submicron technologies."

Pricing and Availability

The TSMC 0.15-, 0.13-micron and 90nm standard cell and I/O libraries' front-end views are available today from Synopsys at www.synopsys.com/dwrequest, to DesignWare library licensees under current maintenance, and back-end views will be available at the end of calendar Q1 2004. TSMC's memory libraries for specific process technologies are expected to be available from Synopsys at the end of calendar Q1 2004 for an additional fee.

About DesignWare

DesignWare, the world's most widely used, silicon proven IP, provides designers with a comprehensive portfolio of synthesizable implementation IP, hardened PHYs and verification IP for ASIC, SoC and FPGA designs. The DesignWare IP family includes industry leading connectivity IP Cores and Verification IP (e.g., USB 1.1, USB 2.0, USB 2.0 PHY, USB 2.0 On-the-Go, PCI, PCI-X, PCI Express, Ethernet, I2C), AMBA™ on-chip bus (logic, peripherals, verification IP) complete Memory solution (e.g., memory controllers, BIST and models), high speed Datapath components, Microcontrollers (8051, 6811) and Star IP processors (e.g., IBM PowerPC® 440, Infineon C166™S and TriCore™1, MIPS32™ 4KE™, NEC V850E™). For a complete directory of Synopsys' available IP visit: www.synopsys.com/ipdirectory. For more information on DesignWare IP, visit: www.designware.com or call 1-877-4BEST-IP.

About TSMC

TSMC is the world's largest dedicated semiconductor foundry, providing the industry's leading process technology and the foundry industry's largest portfolio of process-proven library, IP, design tools and reference flows. The company operates one advanced 300mm wafer fab, five eight-inch fabs and one six-inch wafer fab. TSMC also has substantial capacity commitments at its wholly-owned subsidiary, WaferTech, and its joint venture fab, SSMC. In early 2001, TSMC became the first IC manufacturer to announce a 90nm technology alignment program with its customers. TSMC's corporate headquarters are in Hsinchu, Taiwan. For more information about TSMC please see http://www.tsmc.com/ .

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA) software for integrated circuit (IC) design. The company delivers technology-leading IC design and verification platforms to the global electronics market, enabling the development of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at https://www.synopsys.com/ .

Forward Looking Statements

This press release contains forward-looking statements within the meaning of the safe harbor provisions of Section 21E of the Securities Exchange Act of 1934, including statements regarding the dates of availability of front-end and back-end views of libraries for TSMC's manufacturing processes. These statements are based on Synopsys' and TSMC's current expectations and beliefs. Actual results could differ materially from the results implied by these statements as a result of unforeseen difficulties in completing development of such libraries and optimizing them for Synopsys' design tool flow, as well as other factors contained in Synopsys' and TSMC's reports filed with the Securities and Exchange Commission

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SOURCE: Synopsys, Inc.

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