ARM-Synopsys Verification Methodology Manual for SystemVerilog Endorsed by Leading Japanese Semiconductor Companies

Japanese-Language Edition of the Manual to Be Published by CQ Publishing

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ARM [(LSE: ARM)]; (NASDAQ: ARMHY) and Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that the Verification Methodology Manual (VMM) for SystemVerilog has been endorsed by the Semiconductor Technology Academic Research Center (STARC) and major electronics companies in Japan as a reference to develop advanced verification environments based on the IEEE standard SystemVerilog language. In addition, the companies announced that the Japanese-language edition of the manual will be published by CQ Publishing in Japan. More than 1,800 copies of the English-language edition have been sold to date.

The manual, co-authored by verification experts from ARM and Synopsys, describes how to use SystemVerilog to create comprehensive verification environments using coverage-driven, constrained-random and assertion-based techniques, and specifies library building blocks for interoperable verification components. The VMM for SystemVerilog, reviewed by verification engineers from more than 30 semiconductor industry companies, helps enable chip development teams to achieve measurable functional coverage goals in less time with less effort, giving verification engineers and managers the confidence to tape out complex system-on-chip (SoC) and silicon intellectual property (IP) designs.

"The VMM for SystemVerilog is our recommended reference book to architect SystemVerilog verification environments," said Yoshiharu Furui, senior manager, IP Reuse Engineering Group at STARC Japan. "It defines the state-of- the-art for advanced, coverage-driven functional verification that engineers can use to increase chip development productivity and quality, and will complement the IP Functional Verification Guide being developed by the STARC IP Reuse Engineering Group."

"The VMM for SystemVerilog has been quickly established as an industry- leading reference for advanced verification with SystemVerilog," said Takafumi Nishijima, president, ARM KK. "We welcome STARC's endorsement of this manual and the availability of a Japanese-language edition."

"Companies around the world are adopting SystemVerilog and taking advantage of the advanced methodologies enabled by the language," said Kimio Fujii, president of Nihon Synopsys KK, Synopsys' Japanese subsidiary. "Just as the Reuse Methodology Manual (RMM) for System-on-a-Chip Designs established the open, industry standard for design reuse and reusable silicon IP, the Verification Methodology Manual for SystemVerilog defines an open, industry standard for advanced verification and interoperable verification IP with SystemVerilog.

"The VMM for SystemVerilog will enable all SoC and IP projects to establish an effective, predictable and reusable verification process using SystemVerilog that is based upon the experience of leading industry experts," said Yoshio Takamine, group manager, System Level Design and Verification Technology Development, Renesas Technology Corp.

"The VMM for SystemVerilog will enable any SoC or IP development team to achieve higher levels of verification productivity and quality by providing a standard, interoperable methodology for taking advantage of the coverage- driven, constrained-random techniques used by industry experts," said Zenji Oka, Manager Electronic Devices Company, RICOH COMPANY, LTD.

A free technical tutorial on the VMM for SystemVerilog will be delivered at the EDS Fair in Yokohama, Japan on Friday, January 27, 2006. More information is available at www.vmm-sv.com.

Pricing and Availability

The Japanese-language edition of the VMM for SystemVerilog will be available in February from CQ Publishing for 3,980 yen. For additional information on the Japanese-language edition of the VMM for SystemVerilog and to purchase the English-language edition, please visit: www.vmm-sv.com.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North

America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

About ARM

ARM designs the technology that lies at the heart of advanced digital products, from wireless, networking and consumer entertainment solutions to imaging, automotive, security and storage devices. ARM's comprehensive product offering includes 16/32-bit RISC microprocessors, data engines, 3D processors, digital libraries, embedded memories, peripherals, software and development tools, as well as analog functions and high-speed connectivity products. Combined with the company's broad Partner community, they provide a total system solution that offers a fast, reliable path to market for leading electronics companies. More information on ARM is available at http://www.arm.com/ .

About STARC

The Semiconductor Technology Academic Research Center, STARC, is a research consortium co-founded by eleven major Japanese semiconductor companies* in December 1995. STARC's mission is to contribute the growth of the Japanese semiconductor industry by developing leading-edge SoC design technologies. Currently, STARC is pursuing five objectives toward achieving its mission:

1. Development of technologies for improving design productivity
2. Development of technologies aimed at re-use and sharing of design assets (IP)
3. Development of design technologies to increase the added value of SoC
4. Promotion of collaborative research with universities
5. Training and educational support for engineers and researchers in the semiconductor field

*Founding companies, in alphabetical order: Fujitsu Limited, Matsushita Electric Industrial Co., Ltd., NEC Electronics Corporation, Oki Electric Industry Co., Ltd, Renesas Technology Corporation, Rohm Co., Ltd, Sanyo Electric Co., Ltd, Seiko Epson Corporation, Sharp Corporation, Sony Corporation, Toshiba Corporation. For more information, visit the STARC web site at http://www.starc.jp/ .

Forward Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including expectations of the impact of the Verification Methodology Manual for SystemVerilog on IC design and the adoption of the SystemVerilog language. These statements are based on current expectations and beliefs. Actual results could differ materially from these statements as a result of (i) unforeseen difficulties by customers in completing their SystemVerilog-based designs, (ii) lower-than-expected customer demand for SystemVerilog verification methodologies, (iii) uncertainties attendant to any new technology offering and (iv) certain statements contained in the section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2005 entitled "Management's Discussion and Analysis of Financial Condition and Results of Operations - Factors That May Affect Future Results."

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