Ross Video Selects Synopsys' VCS SystemVerilog Native Testbench to Increase Verification Productivity and Predictability

VCS Native Testbench (NTB) and the Verification Methodology Manual (VMM) for SystemVerilog Help Accelerate Aggressive Verification Schedule

PRNewswire-FirstCall
MOUNTAIN VIEW, Calif.

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that Ross Video, a provider of video production equipment, successfully completed and shipped a major project using Synopsys' VCS® verification solution and its SystemVerilog Native Testbench (NTB) capability to enable faster time-to-market and higher verification predictability. Ross used VCS NTB together with the Verification Methodology Manual (VMM) for SystemVerilog to accelerate the verification schedule of a complex video-processing integrated circuit (IC) that implemented the Warp MD feature in its Synergy MD Series family of multi-definition production switchers.

"Our previous verification methodology relied heavily on the use of hand-written directed tests, followed by extensive lab debug of FPGA prototypes," said Simon Lacroix, hardware developer at Ross Video Limited. "For the Warp MD project, we needed a new verification methodology to handle the increased complexity of the design. We ramped up quickly on SystemVerilog with VCS NTB and used the VMM to help us create a well-structured, scalable testbench environment. The move to SystemVerilog with VCS NTB and the VMM methodology enabled our verification project to be completed a full month ahead of an already aggressive schedule. Deciding to use the VMM was the best thing we could have done."

Moving to the Next Level in Verification Productivity and Predictability

For previous projects, engineers at Ross Video used directed tests combined with C/C++ models of video-processing algorithms to test their designs. While this approach verified the video data path well, it did not provide high coverage of control logic. This meant that control bugs had to be diagnosed in a lab environment on FPGA prototypes -- a multi-day process that was often repeated many times on different design iterations. The iterative nature of this lab-based diagnosis process greatly reduced the predictability of verification schedules.

The Warp MD design included significantly more complex control logic, and thus presented both new challenges and new opportunities to the verification team. Although they had not used constrained-random verification previously, the team had studied the approach and knew that it promised to be the ideal way to address the verification challenge of the new design. After an extensive evaluation to find the best verification language, tools and methodology, the engineers at Ross Video decided to use SystemVerilog for testbench automation with VCS NTB and to follow the VMM methodology. They determined that the VMM provided a clean, modular and elegant approach to verification and that it could be quickly deployed.

The Ross Video team quickly created a robust verification environment utilizing the VMM's built-in self-checking, scenario generation, transaction-level channels, transactors and messaging services. They also made extensive use of SystemVerilog assertions (SVA), both custom-written and selected from the Synopsys SVA assertion-checker library. One of the most valuable features of the resulting environment was the VMM's standardized messaging service. This service provided the team with a standard means of generating, formatting and filtering messages that enabled both design and environment issues to be quickly diagnosed without having to use the waveform viewer. Several of the bugs found with the new environment were in very complex arbitration logic that would have required extensive lab debug resolution time had a purely directed-test approach been used. In the end, the VMM helped to make the verification process more predictable and helped the team finish verification ahead of schedule.

"VCS solution support for SystemVerilog and the VMM methodology enables both new users and experts to dramatically increase verification productivity and shorten chip development schedules," said George Zafiropoulos, vice president of Marketing, Verification Group at Synopsys, Inc. "Ross Video's success with the VCS solution, SystemVerilog and the VMM shows that it is possible to move to the next level in verification productivity and predictability while meeting or beating tough tape-out schedules."

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered

in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http:/www.synopsys.com.

NOTE: Discovery, VCS, Synopsys and are registered trademarks of Synopsys, Inc.

All trade names, trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

Editorial Contacts:
Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Khyati Shah
Edelman
650.429.2769
Khyati.shah@edelman.com

SOURCE: Synopsys, Inc.

CONTACT: Sheryl Gulizia of Synopsys, Inc., +1-650-584-8635, or sgulizia@synopsys.com; or Khyati Shah of Edelman, +1-650-429-2769, or Khyati.shah@edelman.com, for Synopsys

Web site: http://www.synopsys.com/