Synopsys Extends PrimeTime and Star-Rcxt With Statistical Capabilities To Address Variation-Aware Design Challenges

Built on Gold Standards, PrimeTime VX and Star-RCXT VX Tools Deliver Foundation for Comprehensive Variation-aware Design Solution for Sub-65nm Design

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced the latest design-centric offerings in its comprehensive design-for- manufacturing (DFM) solution suite aimed at significantly improving productivity for 65-nanometer (nm) and below IC design. The latest enhancements to the PrimeTime® static timing analysis and Star-RCXT™ extraction tools, PrimeTime VX and Star-RCXT VX, bring the power of statistical analysis to the EDA industry's most widely used and trusted timing sign-off solution. This new capability allows customers to reduce margins, improve design robustness, and enhance parametric yield.

"Synopsys is in a unique position to address the uncertainties of sub-65nm design by providing a comprehensive variation-aware design solution that closes the loop with silicon," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "The breadth of our solution is a result of linking our investments in a number of strategic areas, including test chip technology, process modeling (TCAD), sign-off, and physical implementation, as well as CCS-based statistical library and sensitivity-based parasitic file formats to address emerging design challenges. At the heart of this solution is statistical analysis and extraction technology built on industry standards, which together help to ensure proven accuracy, design flow correlation, and improved productivity."

Statistical-based analysis is emerging as an enabling technology to address uncertainties introduced by the wide variation in device and interconnect performance being observed at sub-65nm technology nodes. Synopsys has taken an evolutionary approach to variation-aware analysis by building this technology on its widely deployed sign-off foundation to preserve customers' investments in their existing flows. Synopsys' variation-aware analysis solution consists of three important ingredients.

First, the Liberty™ Composite Current Source (CCS) modeling technology provides accurate timing models based on device variation. Second, the new Star-RCXT VX package enables sensitivity-based extraction for efficient and accurate parasitic models based on interconnect variation. And third, the new PrimeTime VX package brings together device and interconnect models with statistical timing analysis technology to improve the clarity of timing results for sub-65nm design. Customer results are demonstrating accuracy within 5 percent of HSPICE® simulator and overnight turnaround time for designs as large as three million instances.

"TSMC has been working with Synopsys on variation-aware design," said Ed Wan, senior director, Design Service Marketing at TSMC. "We have tested the accuracy of Synopsys' statistical analysis solution and are encouraged by the results."

"The PrimeTime static timing analysis and Star-RCXT extraction solutions have long been the standard for sign-off in our design flow," said Philippe Magarshack, group vice president and general manager, Central CAD and Design Solutions at STMicroelectronics. "We are pleased with the seamless integration of statistical analysis on this important foundation, enabling the adoption of this emerging technology, that is very much needed for 65nm and 45nm complex SoC designs."

"Our member companies rely on STARC to drive the next level of design productivity required for each successive technology node," said Nobuyuki Nishiguchi, vice president of the Development Department -1 at Semiconductor Technology Academic Research Center (STARC). "A variation-aware design flow is a key component of meeting this goal for 65- and 45-nanometer designs. Synopsys' variation-aware solution delivers the comprehensiveness required to address emerging challenges due to design uncertainties at these small geometries."

In complement to PrimeTime VX and Star-RCXT-VX tools, Synopsys today also announced its comprehensive PrimeYield tool suite for design yield analysis. As the first solution that enables designers to predict and proactively address issues that will impact sub-65nm device manufacturability, PrimeYield links back to design implementation and drives automatic correction within IC Compiler, Synopsys' advanced physical implementation solution. The combination of IC Compiler, PrimeTime VX, Star-RCXT VX and PrimeYield solutions further tightens the link between design and manufacturing to close the loop with silicon (see "Synopsys Extends DFM Leadership with Launch of PrimeYield Tool Suite for Yield Analysis").

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company

delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

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