Synopsys DFT MAX Cuts Test Costs on Nanometer Designs

More Than 50 Tapeouts Prove DFT MAX Reduces Test Time and Cost

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that its DFT MAX scan compression automation solution has been instrumental in reducing test costs related to data inflation on more than 50 successful tapeouts since its general release in September 2005. CSR, Genesis, Micronas, NVIDIA Corporation, and more than 50 other leading semiconductor firms are using this tool to reduce test costs on their nanometer designs. With scores of design projects underway, the DFT MAX tool is fast eclipsing all other scan compression solutions on the market.

"Customers have adopted the DFT MAX solution at a rate that exceeded our expectations," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "Obviously, there was a critical need for a scan compression solution that could significantly reduce costs related to inflation of test data. But it needed to be easy to use, with low impact on downstream flows. We believe ease-of-use combined with quality-of-results is what our customers care about most, and they're telling us 'You got it right with the DFT MAX solution.' "

With the advent of nanometer processes, designers are generating more test patterns to meet their high quality goals. In addition, the amount of data needed for each test pattern increases because the number of internal scan registers increases with circuit complexity. The DFT MAX solution reduces costs associated with test data inflation by performing on-chip compression to reduce by 10-50 times the volume of information to be stored in tester memory. DFT MAX avoids costly reloading of test patterns on the tester and allows designers to use more patterns to achieve higher test quality. The tool also reduces test application time by 10-50 times.

"High-volume manufacturers are looking at ways to manage higher costs at the tester that stem from test data volume inflation," said Graham Etchells, director of Test Marketing, Synopsys Implementation Group. "The DFT MAX solution helps offset these higher costs, providing customers maximum utilization of their tester assets. More than 50 leading semiconductor firms worldwide are using this tool to reduce test costs. Given this success, we believe the DFT MAX tool will soon become the de facto standard for scan compression."

Using the DFT MAX solution requires no expertise in test compression techniques. Its gates-only adaptive scan architecture is the most area-efficient solution available. By avoiding the use of complex sequential state machines for compression-decompression, the adaptive scan architecture disperses test logic throughout the design, alleviating wire-routing congestion and reducing silicon area overhead cost. Working seamlessly within Synopsys' Galaxy™ design platform, DFT MAX produces predictable results with virtually zero impact on timing. The Galaxy platform delivers design engineers a single environment for synthesis, physical implementation, and sign-off. Concurrent optimization for timing, signal integrity, area, power, and test within the Galaxy environment helps eliminate costly and time-consuming design iterations between front-end and back-end flows.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

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