Synopsys to Acquire HPL Technologies, Inc.

Acquisition Will Establish EDA Industry's First Direct Connection into Fabrication Processes

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced it has signed a definitive agreement to acquire HPL Technologies, Inc. (OTC: HPLA.PK), a leader in yield management software and test chip solutions. The acquisition solidifies Synopsys' position as the leading EDA vendor in design for manufacturing (DFM), and the first with a comprehensive design-to-silicon flow that links directly into the semiconductor manufacturing process. Integrating HPL's yield management and test chip technologies into Synopsys' industry-leading DFM portfolio will enable customers to increase productivity and improve profitability in the design and manufacture of advanced semiconductor devices. Synopsys will also broaden its DFM research and development expertise by integrating HPL's team of experienced engineers.

Under the terms of the agreement, Synopsys will acquire HPL for approximately $13 million, or $0.30 per share. The all-cash transaction, which will require HPL shareholder approval, is expected to close during Synopsys' first quarter of fiscal 2006 and is subject to customary closing conditions.

"With the addition of this critical piece of the DFM solution, Synopsys will help customers close the productivity gap and increase profits by optimizing yield and shortening design-to-manufacture time," said Anantha Sethuraman, vice president of DFM for Synopsys' Silicon Engineering Group. "Today, the typical design-to-manufacturing cycle takes 18 to 20 months. By linking directly into the fab, Synopsys can help significantly reduce the time between concept and manufacturing, and accelerate the introduction of new designs."

Synopsys' DFM solution reaches beyond the traditional boundaries of EDA by identifying and addressing manufacturing problems early in the design process, all the way from place and route through to physical verification (RET -- reticle enhancement technology), mask optimization and process tuning (TCAD). By integrating HPL into its DFM solution, Synopsys will deepen its connection to the fab and obtain direct access to the yield data needed to reduce systematic defectivity.

HPL provides customizable software products, TestChip IP and patented RDOM technologies that enable customers such as integrated device manufacturers (IDMs), fabless semiconductor companies and foundries to quickly identify and correct yield-limiting factors in their design, technology development and manufacturing processes. HPL's tools analyze parametric, bin/sort, bitmap, MES, defect and design data as well as monitor the changes made to the process recipes resulting in expedited yield learning and yield improvement.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http:/www.synopsys.com.

Forward Looking Statements

This press release contains forward-looking statements within the meaning of the safe harbor provisions of Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected benefits and timing of Synopsys' acquisition of HPL Technologies. These statements are based on Synopsys' current expectations and beliefs. Actual results could differ materially from these statements as a result of unforeseen difficulties in integrating HPL's solutions into Synopsys' product portfolio and certain statements contained in the section of Synopsys' Quarterly Report on Form 10-Q for the fiscal quarter ended July 31, 2005 entitled "Factors That May Affect Future Results."

NOTE: Synopsys is a registered trademark of Synopsys, Inc. Any other trademarks mentioned in this release are the intellectual property of their respective owners.

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