Top Layer Networks Uses Synopsys' Testbench Automation Solution to Verify Network Security Chip

Vera Tool Offers the Thorough Verification Necessary for Mission-Critical Network Protection

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that Top Layer Networks, a global leader for high-performance intrusion-prevention solutions, used Synopsys' Vera® testbench automation tool to verify the chip at the heart of the Attack Mitigator IPS 5500 family of intrusion prevention solutions (IPS). The advanced features of the Vera tool and Synopsys' proven Reference Verification Methodology (RVM) enabled the Top Layer team to improve its process for detecting and fixing design bugs before tapeout to ensure the integrity of the final product.

"There was no doubt that Synopsys' Vera testbench automation solution was the right choice for our verification environment," said Jay Brown, verification manager at Top Layer. "Our customers rely on our products to safeguard their networks from zero-day exploits, denial-of-service (DoS) attacks, worms, spyware, email viruses and other threats. The thorough verification provided by the Vera tool and the RVM allowed us to design an industry-leading product that helps prevent malicious content from slipping through the cracks."

In order to improve their traditional VHDL-based approach, Top Layer evaluated competing testbench automation solutions in the market. They selected the Vera tool for several key reasons, including its superior support for constrained-random stimulus generation, functional coverage and other advanced verification methods. They also chose the Vera tool for its extensive RVM guidelines and documentation, which allow faster setup of the verification environment. Synopsys' support for SystemVerilog, including assertions, coverage and testbench capabilities, was also a key factor in the decision since this standard will be important for future Top Layer projects.

By following the RVM guidelines and leveraging the base-class library provided by Synopsys, the Top Layer engineers were able to set up and leverage their complete verification environment in only three months. Although the Attack Mitigator IPS 5500 design was their first project using a hardware verification language or constrained-random stimulus generation, the team was able to learn the new techniques quickly and apply them effectively for thorough chip verification.

"The experience of Top Layer Networks shows how much value the tools and bug-finding technologies in the Discovery™ Verification Platform bring to our customers even from the very first usage," said Farhad Hayat, vice president of Marketing, Synopsys Verification Group. "This value is passed on to their customers, who benefit from a level of product reliability and robustness that can only be achieved with a thorough verification process."

Founded in 1997, Top Layer Networks develops network security solutions that enable enterprises worldwide to protect their infrastructure and critical online assets from cyber-threats. The Company's patented, ASIC-based products are engineered to deliver accurate and reliable protection mechanisms while operating as robust in-line network security devices.

Synopsys Discovery Verification Platform

The Discovery Verification Platform is a unified environment that provides high performance and efficiency of interaction among all platform components, including mixed-HDL simulation, mixed-signal, system-level verification, assertions, DesignWare® verification intellectual property, code coverage, functional coverage, testbenches and formal analysis. Combined with support for industry standard hardware design and verification languages, including Verilog, VHDL, SystemVerilog, SystemC™ and OpenVera®, and Synopsys' proven RVM, the Discovery Verification Platform helps designers achieve higher levels of verification productivity by contributing to first-time silicon success within required project cycles.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at https://www.synopsys.com/ .

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SOURCE: Synopsys, Inc.

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