Synopsys' DFT MAX Reduces Test Costs on NVIDIA Graphics Processing Units

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that NVIDIA Corporation, a worldwide leader in graphics and digital media processing, has adopted the Synopsys DFT MAX Test Synthesis with Adaptive Scan technology for its next-generation graphics processor chips. Reducing test costs while improving test quality was a driving factor in the adoption of DFT MAX. Proven on multiple 130-nm, 90-nm, and 65-nm designs, DFT MAX consistently delivers predictable test cost reduction in an easy-to-use synthesis solution.

"We began working closely with Synopsys on advanced test synthesis and test compression technologies after encountering the limitations of traditional test methodologies as applied to our high-volume, high-performance products," said Dan Smith, director of hardware engineering at NVIDIA Corporation. "In order to test for transition and bridging on our sophisticated graphic processors in 130-nm, 90-nm and smaller process geometries, we required the Adaptive Scan technology in DFT MAX. Using DFT MAX as part of our Design Compiler® synthesis flow reduced expensive test time and data volume by 10x without adversely affecting our strict timing requirements."

Working seamlessly with the Design Compiler flow, DFT MAX predictably reduces test costs by up to 50x compared with traditional scan techniques. The key advantage of DFT MAX is that it is easy to implement and is far less intrusive on design flows and design performance than alternative solutions. Design Compiler and DFT MAX are an integral part of Synopsys' Galaxy™ Design Platform, which gives engineers a single design environment for synthesis, physical implementation, and sign-off. Concurrent optimization for timing, area, power, and test within the Galaxy environment eliminates costly and time-consuming design iterations between front-end and back-end flows.

"At Synopsys, we continually focus on improving our tools and flows to increase customer productivity and lower their costs of design and test," said Graham Etchells, director of marketing, Synopsys Implementation Group. "DFT MAX is a prime example of this focus. It delivers the significant test cost reduction needed for today's designs, while providing compression that's easy to implement due to its seamless integration with the Design Compiler flow. We are encouraged to have NVIDIA as one of our early customers deploying this unique capability on highly complex graphics processor designs."

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http:/www.synopsys.com .

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