Synopsys Continues IC Compiler Momentum With 2006.06 Release

Release Brings New Advances in Yield, Low Power, and Testability

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced the 2006.06 release of IC Compiler, Synopsys' next-generation place- and-route solution. The 2006.06 release delivers advances in the areas of integrated design planning, enhanced physical test, advanced low-power design, true concurrent multi-corner/multi-mode optimization, and design-for-yield techniques. This release continues the momentum initiated by the introduction of the IC Compiler solution in June 2005. Since then, IC Compiler has steadily drawn customers from a broad class of applications, from cost-conscious 180- and 130-nanometer (nm) designs to performance-driven 65-nm designs. Several of these prominent customers are scheduled to detail their tapeout experiences using IC Compiler at the Design Automation Conference in San Francisco next month.

"IC Compiler has seen strong support among our key customers who have a diverse family of designs and are often at the leading edge in adopting new technology," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "Synopsys holds leading technology positions in physical design, optimization, sign-off and design-for-manufacturing (DFM), and we are bringing these technologies together to make IC design more efficient. The 2006.06 release is yet another example of continued technology delivery and further distances IC Compiler from the field."

The 2006.06 release allows flat floorplan creation and refinement in the same environment as physical implementation -- placement, clock tree, and routing. These capabilities utilize proven technologies from the JupiterXT™ tool for floorplanning, automatic high-quality macro placement, and automatic power-network synthesis and analysis. The integration brings about commonality in graphical user-interface, timing analysis, placement, and global routing technologies, to drive higher-quality floorplanning and faster time to results.

The 2006.06 release also includes enhanced capabilities for low-power design, manufacturing testability and design-for-yield (DFY). It provides improvements in multi-Vt leakage power optimizations as well as advanced leakage management with MTCMOS power-gating. The release introduces a new syntax for capturing power-domain specifications and enhances Synopsys' Liberty™ library format for MTCMOS power modeling. Also included is the SCANDEF-based interface to RTL-based scan synthesis using DFT MAX, and integrated support for scan-chain repartitioning and reordering to reduce congestion and improve routability. In the area of DFM, the 2006.06 release adds to the existing set of capabilities for impacting yield during design, including intelligent multi-pattern via optimization, timing-driven wire spreading, timing-driven metal fill, and critical area analysis. New capabilities include timing-driven via redundancy, staggered metal fill, and timing-driven half-pitch wire spreading after detail route. Another key new capability in limited customer availability is lithography hot-spot fixing.

Today, many advanced designs need to operate in several different functional modes. In addition, deep-submicron geometries require designs to be characterized across multiple process corners. A key requirement arising from these factors is the ability to concurrently optimize across multiple modes and corners. The 2006.06 release of IC Compiler brings this capability into general availability. In addition, the release provides early support for signoff-driven closure for advanced designs, bringing in exact sign-off data from incremental runs of the PrimeTime® static timing analysis and Star- RCXT™ extraction tools. Used together, true concurrent multi-mode/multi- corner optimization and sign-off driven closure provide a big boost in designer productivity for advanced designs.

The IC Compiler 2006.06 release is available immediately.

About IC Compiler

IC Compiler is Synopsys' next-generation place-and-route system. It provides superior results and faster time-to-results by extending physical synthesis to full place-and-route, and by enabling signoff-driven design closure. Current-generation solutions have a limited horizon because placement, clock tree, and routing are separate, disjointed operations. IC Compiler's Extended Physical Synthesis (XPS) technology breaks down the walls between these steps by extending physical synthesis to full place-and-route. IC Compiler has a unified, TCL-based architecture that implements innovations and harnesses some of the best Synopsys core technologies. It is a complete place- and-route system with everything necessary to implement next-generation designs, including physical synthesis, placement, routing, timing, signal integrity (SI) optimization, power reduction, design-for-test (DFT), and yield optimization.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company

delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the anticipated rate of customer adoption of Synopsys' IC Compiler product. These statements are based on current expectations and beliefs. Actual results could differ materially from these statements as a result of the features and pricing of competitors' product offerings, unforeseen difficulties of customers in implementing their design using IC Compiler, uncertainties attendant to any new product offering and certain statements contained in the section of Synopsys' Quarterly Report on Form 10-Q for the fiscal quarter ended April 30, 2006 entitled "Management's Discussion and Analysis of Financial Condition and Results of Operations - Factors That May Affect Future Results."

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