Synopsys Extends DFM Leadership With Launch of PrimeYield Tool Suite for Yield Analysis

Integration of Production-Proven Design and Manufacturing Technology Accelerates Time to Yield

In a move that empowers integrated circuit (IC) designers by giving them more control over the manufacturability of their leading-edge designs, Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today launched the PrimeYield tool suite. Built for 65 nanometer (nm) and smaller technology nodes, PrimeYield integrates design with manufacturing by accurately predicting design-induced mechanisms that threaten manufacturing tolerances and by providing automated correction guidance to upstream design implementation tools.

Developed in close collaboration with customers and partners, the PrimeYield solution is built on production-baseline technology and manufacturing models used by the leading foundries and integrated device manufacturers (IDMs). By empowering designers with a tool that can predict and correct manufacturing-sensitive design patterns before tapeout -- thus preventing such problems from threatening manufacturing tolerances -- PrimeYield gives designers improved control over the manufacturability of their advanced 65nm designs. In turn, manufacturers are able to improve process efficiencies and minimize yield loss. The result is accelerated time- to-production and time-to-market for leading-edge devices.

PrimeYield gives designers a preview of the issues that will impact the manufacturability of their devices at 65nm and below, along with a quick and easy means of correcting them using links to design implementation. This gives designers the critical toolset to correct and modify the design before tapeout.

At 65nm and below, chip production is highly sensitive to process issues, such as lithography errors, chemical-mechanical polishing (CMP) and particle- induced defects. To address these critical issues, the PrimeYield tool suite includes the following modules: lithography compliance checking (LCC), which flags potential lithographical errors and process-variation effects for the designer earlier in the design process; model-based CMP, which locates and analyzes uneven metal fill, a major source of systematic failures in advanced chip designs; and critical area analysis (CAA), which enables analysis and improvement of critical areas with higher probability of yield loss in the design layout.

In addition to providing high accuracy, PrimeYield is tightly linked to design implementation. PrimeYield drives automatic correction within Synopsys' IC Compiler advanced physical implementation solution and accurate parasitic extraction within the Star-RCXT™ tool. Enhancements to the Star- RCXT extraction tool and the Synopsys PrimeTime® static timing analysis tool were also announced today, further strengthening the link between design and manufacturing to help optimize yields at 65nm and below. These latest enhancements to the industry's most widely used and trusted timing sign-off solution will allow customers to improve design robustness and parametric yield.

"TSMC and Synopsys are accelerating time-to-production by collaborating closely on DFM technologies to enhance advanced design flows," stated Ed Wan, director of Design Service Marketing, TSMC. "PrimeYield uses TSMC's DFM information to analyze yield problems and drive implementation tools to fix those problems."

Citing PrimeYield as the latest tool in its comprehensive DFM solution suite, Raul Camposano, Synopsys' chief technology officer, senior vice president and general manager of Silicon Engineering Group, commented, "High accuracy and fast turnaround time are the cornerstone of our promise to enable predictable success for our customers. With its ability to help predict and prevent critical problems before they become a production threat, PrimeYield gives designers more control over the manufacturability of their designs. As the newest component of our DFM solution set, we believe it will further enable our customers to improve their device performance and accelerate their time to production. With these advantages, we are helping them meet tight market windows, thereby enhancing their profitability."

PrimeYield list pricing starts at $225,000 per module.

About Synopsys DFM

With its DFM tools, Synopsys is expanding on what is already the industry's most comprehensive design for manufacturing (DFM) solution that spans from RTL to silicon. Synopsys' DFM product family addresses critical manufacturability and yield issues with the following products: IC Compiler physical design solution, PrimeYield LCC, PrimeYield CMP and PrimeYield CAA technologies, Hercules™ physical verification tool, Proteus OPC, CATS® mask data preparation product, SiVL® lithography verification tool, patented PSM technology, and physics-based TCAD suite of simulation products. Synopsys' Manufacturing Yield Management (MYM) solutions extend directly into the fab, providing customers real time access to yield data and the analysis capability needed to reduce random, systematic and parametric defects.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at https://www.synopsys.com/.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the anticipated benefits of Synopsys' PrimeYield tool suite. These statements are based on current expectations and beliefs. Actual results could differ materially from these statements as a result of unforeseen difficulties of customers in deploying the tool suite, uncertainties attendant to any new product offering and certain statements contained in the section of Synopsys' Quarterly Report on Form 10-Q for the fiscal quarter ended April 30, 2006 entitled "Management's Discussion and Analysis of Financial Condition and Results of Operations - Factors That May Affect Future Results."

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