Micronas Tapes out HDTV Chip With Synopsys' IC Compiler

IC Compiler Reduces Chip Cost by Achieving Over 90% Area Utilization

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that Micronas (SWX: MASN) has taped out one of its advanced HDTV (high-definition television) chips using Synopsys' IC Compiler physical implementation solution. This new chip is a key part of Micronas' drive to improve picture and sound quality for flat-panel TV and to provide benefits to manufacturers in the total cost structure from R&D to production, based on very high integration. The price-performance pressures associated with this intensely competitive market put extreme requirements on chip design, requiring the highest silicon utilization (i.e., smallest possible die size) without compromising processing performance. Using the Galaxy™ design platform with new IC Compiler optimization technology, Micronas was able to tape out this design at the required performance while achieving a remarkably high utilization in excess of 90 percent.

"IC Compiler's highly efficient optimization technology was critical in helping us achieve our objectives for die-size and component cost," said Dirk Wieberneit, vice president, Product Development, Consumer at Micronas. "We have decided to standardize on the Galaxy platform for all our design work because we've found that its close integration of tools, algorithms, and libraries has increased the efficiency of our teams and helped to lower our overall cost of design."

The IC Compiler solution's unique Extended Physical Synthesis (XPS) technology was a major factor in enabling Micronas to achieve both the performance and cost goals of this project. XPS is the architecture that increases IC Compiler efficiency by combining synthesis, placement, clock and routing in a unified optimization environment. Another element used by Micronas to reduce the die size was IC Compiler's new congestion-reduction algorithm that automatically resolves local congestion hot-spots and increases the maximum achievable utilization. Micronas also applied Synopsys' design- for-test (DFT) solution successfully for maximum efficiency. The DFT MAX tool was used to automatically implement test compression that can reduce testing costs by up to 50X with minimal area overhead. This design also benefited from IC Compiler's physical test optimization techniques, including scan chain repartitioning and reordering for reduced congestion.

"Micronas has been a major strategic customer for Synopsys and was an early adopter of our new technologies, including DFT MAX and IC Compiler," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "This tapeout and the impressive overall results are a strong endorsement of the depth of Synopsys technology and Micronas' design expertise."

About IC Compiler

The IC Compiler tool is Synopsys' next-generation physical implementation system. It provides superior results and faster time-to-results by extending physical synthesis to full place-and-route, and by enabling signoff-driven design closure. Current-generation solutions have a limited horizon because placement, clock tree, and routing are separate, disjointed operations. IC Compiler's Extended Physical Synthesis (XPS) technology breaks down the walls between these steps by extending physical synthesis to full place-and-route. IC Compiler has a unified, TCL-based architecture that implements innovations and harnesses some of the best Synopsys core technologies. It is a complete place-and-route system with everything necessary to do next-generation designs, including physical synthesis, placement, routing, timing, signal integrity (SI) optimization, power reduction, design-for-test (DFT), and yield optimization.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at www.synopsys.com.

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SOURCE: Synopsys, Inc.

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