Synopsys IC Compiler Enables Toshiba's Tape Out of High-Performance 90-nm Consumer Wireless Chip

Concurrent Multi-Mode Optimization Speeds Timing Closure

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that Toshiba Corporation (TSE: 6502), a leading supplier of semiconductors, has used the Synopsys IC Compiler next-generation physical implementation solution to successfully tape out its next-generation TC90515XBG home digital network chip. Compared to its predecessor, the TC90515XBG delivers higher performance and increased functionality with reduced die-size and lower power consumption. The ability to use IC Compiler to concurrently optimize the design across all five of its operating modes was a critical factor in Toshiba's ability to meet its aggressive performance goals. IC Compiler was also able to significantly speed Toshiba's time-to- results due to its unified user environment for all design steps from prototype floorplanning through final chip finishing. Toshiba was able to further reduce the cost of the design by adopting Synopsys' DFT MAX adaptive scan technology to reduce chip testing time.

"We were impressed by our early results with IC Compiler and decided to use it for the complete physical design of the TC90515XBG," said Dr. Tohru Furuyama, general manager of the Center for Semiconductor Research and Development, Toshiba Corporation. "We found that IC Compiler met our expectations, allowing us to design a highly differentiated SoC while meeting our delivery schedule."

Toshiba's TC90515XBG is a 90-nanometer (nm), high-performance wireless chip for consumer networks. It has a dual MeP core architecture that supports all IEEE 802.11 wireless LAN standards; MPEG-2 TS, PCI, I2C and IR (Infra-Red) interfaces; and content protection with DTCP-IP. The chip has two functional modes at 200MHz and 80MHz and 3 test modes all of which were optimized concurrently by IC Compiler to give significant improvements in hold-time fixing and reduced margin. IC Compiler also helped reduce the chip's leakage power by optimizing the trade-off between high-speed and low-power cells.

"IC Compiler and the Galaxy™ platform allowed us to significantly accelerate our time to results," said Takashi Yoshimori, technology executive of SoC Design, Semiconductor Company, Toshiba Corporation. "IC Compiler gave our designers a comprehensive solution for physical design with one set of libraries and constraints, a single-user environment, and support for physical test and power optimization. In addition, we found the tight correlation to sign-off with PrimeTime® SI to be a key contributor to faster design closure."

Toshiba found that new optimizations within IC Compiler, combined with extensive analysis capabilities, were easy to use and shortened their time to results. IC Compiler's completeness allowed Toshiba to use the same tool for all physical implementation steps from initial prototyping to final finishing. Toshiba was able to achieve over 80 percent area utilization, power-network voltage drop of less than 25 millivolts and over 80 percent low-leakage (high Vt) cells for improved leakage-power dissipation.

"Toshiba has long been a key customer and an early adopter of our most advanced technologies, such as IC Compiler and DFT MAX. The results achieved with the TC90515XBG chip are clear evidence of the success of our close collaboration," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "We value Toshiba's input in guiding our products and look forward to working with them on future advanced designs."

About IC Compiler

IC Compiler is Synopsys' next-generation physical implementation solution. It provides superior results and faster time-to-results by extending physical synthesis to full place-and-route, and by enabling signoff-driven design closure. Current-generation solutions have a limited horizon because placement, clock tree, and routing are separate, disjointed operations. IC Compiler's Extended Physical Synthesis (XPS) technology breaks down the walls between these steps by extending physical synthesis to full place-and-route. IC Compiler has a unified, TCL-based architecture that implements innovations and harnesses some of the best Synopsys core technologies. It is a complete place-and-route system with everything necessary to do next-generation designs, including physical synthesis, placement, routing, timing, signal integrity (SI) optimization, power reduction, design-for-test (DFT), and yield optimization.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the

global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at www.synopsys.com .

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