Synopsys' TetraMAX ATPG Delivers Significant Productivity Gains for Designers

TetraMAX® ATPG Performance Speedup Combined with a New Waveform Debugger Streamline Test Pattern Generation for Complex Designs

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced enhancements to the TetraMAX® test solution that provide designers with significant productivity gains for both automatic test pattern generation (ATPG) and test debugging tasks. Enhancements result in a typical speedup of four times (4x) or more in ATPG runtime performance across all design styles compared with the previous software release. TetraMAX ATPG also includes a new waveform debugger. Together, these new capabilities offer substantial productivity benefits for designers faced with the challenge of creating high-quality manufacturing tests for complex ICs.

Increased design complexities combined with stringent test quality requirements are driving the need to target manufacturing defects more efficiently. Designers can now take advantage of TetraMAX ATPG's 4x speedup in runtime performance to achieve higher test quality in a shorter amount of time. Designers gain additional productivity using TetraMAX ATPG's new waveform debugger, which lets designers debug test design rule violations and test protocols much more efficiently. These enhancements provide designers improved runtime performance and debugging capabilities needed to create the highest quality tests.

"Efficient test pattern generation helps minimize the time and effort it takes to deliver our advanced SoC and microcontroller solutions," said Osamu Tada, department manager of System Level Design and Verification Technology Department at Renesas Technology Corp., Japan's largest semiconductor manufacturer. "We are very encouraged that this significant ATPG run-time improvement has the potential to further reduce time-to-volume for our products."

"We observed more than a 6x performance speedup, compared with the 2004.12 release, when we ran the latest version of TetraMAX ATPG for transition delay tests," said Bruno Latulippe, DFT manager at Tundra Semiconductor Corp., which designs standards-based System Interconnect for use by the world's leading communications and storage system companies. "As the complexity of our product portfolio increases, we anticipate this substantial boost in ATPG throughput will help us expedite the time it takes to implement at-speed testing."

"Faster debugging reduces time-to-results, especially for circuits that utilize complex initialization sequences and scan protocols," said Graham Etchells, director of marketing, Synopsys Test Automation Business Unit. "TetraMAX ATPG's new waveform debugger helps designers quickly isolate and correct the causes of design-for-test problems that tend to create project bottlenecks."

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http:/www.synopsys.com .

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