Synopsys Unveils NanoTime Next-Generation Transistor-Level Static Timing Analysis Solution

NanoTime Extends Synopsys' Leadership in Transistor-Level Simulation and Analysis

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced the availability of NanoTime, a next-generation transistor-level static timing analysis solution that delivers concurrent timing and signal integrity (SI) analysis to address emerging custom circuit design challenges. NanoTime also delivers a significant performance and capacity boost to analyze complex transistor circuits overnight with HSPICE® accuracy. Its seamless integration with PrimeTime® static timing analysis solution enables chip- level analysis of designs that includes both gate- and transistor-level blocks. NanoTime is a new addition to Synopsys' comprehensive circuit simulation and analysis product portfolio that includes NanoSim®, HSIM® and HSPICE tools for circuit simulation, and ESP-CV for symbolic simulation.

"We have been successfully using Synopsys' PathMill® transistor level static timing analysis solution over the past decade for silicon-accurate analysis on a variety of ARM® processors, including ARM7™, ARM9™ and ARM10™ processor families," said Keith Clarke, vice president of Technical Marketing, ARM. "Now, with NanoTime, we believe we can achieve higher predictability and greater productivity over PathMill. NanoTime not only recognizes our custom design structures, but also offers HSPICE correlation. We are currently incorporating NanoTime in our 90-nanometer design flow."

NanoTime offers higher predictability and improved productivity to custom designers over existing solutions. Its concurrent timing and SI features enable designers to accurately and quickly identify timing issues early and avoid expensive silicon re-spins. With a superior ability to recognize complex custom design structures and its embedded NanoSim technology for dynamic circuit evaluation, it helps ensure silicon-accurate analysis. NanoTime delivers the performance and capacity required to perform overnight analysis of complex circuits with over one million transistors. Designers' productivity is further boosted by significant ease-of-use features, including interactive static timing analysis, extracted timing model (ETM) creation, and seamless integration with PrimeTime chip-level analysis tool.

"Synopsys' comprehensive circuit simulation and analysis product family has been deployed in the most demanding microprocessor, DSP and memory designs for the last decade," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "Our customers are seeking solutions that offer higher productivity and better predictability in their custom design flows. With the introduction of NanoTime, we deliver a comprehensive transistor-level analysis solution that addresses our customers' most demanding requirements."

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http:/www.synopsys.com.

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