Silicon Logic Engineering Reduces Verification Development Time Using Synopsys' Reference Verification Methodology With VCS and Vera Solutions

ASIC and System Developer Adopts Synopsys' Discovery™ Verification Platform for 90-Nanometer Chip

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that Silicon Logic Engineering (SLE), a provider of high-end ASIC and system design services, has adopted Synopsys' VCS ® comprehensive RTL verification solution and Vera® testbench automation tool to accelerate its chip development process. SLE is taking advantage of the Synopsys Reference Verification Methodology (RVM) to reduce the development time for its verification environment and to ensure the highest-quality verification results. In addition to the VCS solution and Vera tool, SLE has adopted Synopsys' Magellan™ hybrid formal analysis, Leda® RTL checking and Formality® formal equivalency checking solutions from the Discovery™ Verification Platform.

"We chose Synopsys as our verification partner on our latest 90-nanometer, 40-million-gate chip development project after evaluating several providers," said Bob Solberg, vice president of Operations and co-founder at SLE. "Synopsys was able to deliver the breadth of tools, proven methodology and responsive support we needed to be confident in our aggressive schedule and quality targets. In particular, Synopsys' RVM enables us to cut our verification development time, while promoting industry best practices within our verification team. The collaborative relationship we have with the Synopsys teams was also a significant factor in our decision making process. "

The Synopsys Reference Verification Methodology, delivered with VCS Native Testbench technology and the Vera tool, helps engineers to quickly implement and deploy advanced verification environments using modern constrained-random, coverage-driven and assertion-based verification techniques. The RVM speeds verification development by providing pre-defined base-class libraries with advanced features for transaction modeling, transactor construction, messaging services, verification flow, assertion checkers, and more. In addition, Synopsys provides extensive RVM documentation and offers training to enable both small and large chip development teams to quickly implement industry best practices for verification.

"Synopsys' RVM enables chip developers to rapidly adopt the proven verification techniques used by the experts," said Farhad Hayat, vice president of Marketing, Verification Group, Synopsys, Inc. "With support in the Vera tool and in VCS Native Testbench technology for even higher performance, the RVM enables ASIC and system developers such as SLE to complete their projects with a higher level of verification confidence in less time."

SLE (www.siliconlogic.com) specializes in right-first-time, leading edge, digital Application Specific Integrated Circuits (ASIC) and system design services. SLE's proven and repeatable Think Physical™ design process, tools, and semiconductor intellectual property reduce time-to-market and are provided by one of the most experienced VLSI design teams in the industry.

Synopsys Discovery Verification Platform

The Discovery Verification Platform is a unified environment that provides high performance and efficiency of interaction among all platform components, including mixed-HDL simulation, mixed-signal, system-level verification, assertions, DesignWare® verification intellectual property, code coverage, functional coverage, testbenches and formal analysis. Combined with support for industry-standard hardware design and verification languages, including Verilog, VHDL, SystemVerilog, SystemC™ and OpenVera® and Synopsys' proven Reference Verification Methodology, the Discovery Verification Platform helps designers achieve higher levels of verification productivity by contributing to first-time silicon success within required project cycles.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at https://www.synopsys.com/ .

NOTE: DesignWare, Leda, Formality, OpenVera, Vera and VCS are registered trademarks of Synopsys, Inc. Discovery and Magellan are trademarks of Synopsys, Inc. All other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

CONTACT:
Isela Warner
Synopsys, Inc.
+1-650-584-1644
igamboa@synopsys.com

Sarah Seifert
Edelman
+1-650-968-4033
sarah.seifert@edelman.com

SOURCE: Synopsys, Inc.

CONTACT: Isela Warner of Synopsys, Inc., +1-650-584-1644, or igamboa@synopsys.com; or Sarah Seifert of Edelman, +1-650-968-4033, or sarah.seifert@edelman.com, for Synopsys, Inc.

Web site: http://www.siliconlogic.com/

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