Synopsys Delivers First 65-nm Reference Flow for IBM, Samsung and Chartered

Common Platform Technology Reference Flow Adds Critical Area Design-for-Manufacturing Capability in IC Compiler

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced availability of its extended RTL-to-GDSII low-power reference design flow for the latest 65-nanometer (nm) process offered by the IBM-Chartered Semiconductor Manufacturing-Samsung Common Platform technology initiative. The 65-nm reference flow addresses complex design rules and directly analyzes and reduces critical areas during the implementation process. Reducing these critical areas in a chip leads to higher yields and lower chip costs. Synopsys' flow is the first reference flow for the Common Platform technology's 65-nm offering.

"Synopsys' delivery of the first complete reference flow for the CMOS 10LP process is an important milestone in making the 65-nanometer Common Platform manufacturing capabilities available to the chip design community," stated Dr. Ben Suh, vice president, ASIC & Foundry Business Development, System LSI division at Samsung Electronics. "The support for 65-nanometer design rules and critical area reduction capabilities that Synopsys' IC Compiler physical implementation solution brings to the reference flow are important to our foundry customers. Samsung Electronics has worked closely with Synopsys to establish this vital link between design intent and manufacturing in the Common Platform 65-nanometer ecosystem."

As a key part of the Synopsys reference flow, IC Compiler anticipates the manufacturing process to reduce random yield loss due to particulate contamination. Using Critical Area Analysis (CAA) algorithms and foundry- supplied data, IC Compiler analyzes and reports areas in the design that will be most sensitive to yield loss caused by random particles. IC Compiler uses an automated wire-spreading methodology to reduce total critical area while preserving timing, power, and other design constraints. The Common Platform foundries analyzed the impact of IC Compiler and found that it resulted in a material reduction in total critical area. The ability to reduce critical area during the implementation process is important to reducing total design time because it helps eliminate multiple design iterations that can result when using uncorrelated tools.

"Synopsys has worked closely with all three Common Platform technology member foundries to address manufacturability issues by defining advanced router rules and extending and optimizing a process-aware reference flow for higher yields," said Steve Longoria, vice president, Semiconductor Technology Platform for IBM Technology Collaboration Solutions. "The optimization of reference flows and IP to a process technology has become increasingly important in ensuring customer design success as technology offerings expand into the 65-nanometer realm."

The new 65-nm process technology adds a variety of new design rules that must be satisfied during the design process. The Common Platform technology companies have generated new design rules to reduce systematic yield loss and improve reliability at the 65-nm node. Synopsys' IC Compiler and Astro™ physical design tools support these new rules during the implementation process and Hercules™ DRC thoroughly checks them during the physical verification process. The Common Platform technology companies also supply the necessary CMOS 10LP technology files and DRC rule decks to their customers.

The Synopsys Common Platform 65-nm reference flow uses advanced methodologies to take the designer through each step of the design process while maintaining data consistency through the Milkyway™ database and shared design constraint files. The flow allows designers to easily and accurately maintain process technology files, memories and standard cell and I/O libraries, and design data in a single consistent directory structure. The reference flow, which can be extended and enhanced by designers to address design-specific requirements, is compatible with the Synopsys Pilot Design Environment that is used by Synopsys Professional Services for its customer design projects and has been deployed to numerous leading semiconductor companies. The full Synopsys RTL-to-GDSII flow has been validated by Chartered, IBM, and Samsung using ARM® Metro™ low-power products, part of its Artisan® physical IP family. Customers around the world are using earlier versions of the Synopsys Common Platform technology reference flow to design 90-nm chips.

"Our work with Synopsys on its reference flow supports the needs of our customers targeting the 65-nanometer Common Platform technology process. The complete and consistent flow addresses designers' needs for quickly meeting area, performance, power, signal integrity, and DFM goals," said Kevin Meyer, vice president of Worldwide Marketing and Platform Alliances at Chartered. "We worked with Synopsys to validate the various data models and flows and demonstrate the flow's quality-of-results and ease-of-use. Our rigorous independent internal testing has allowed us to fully qualify this flow for use with our 65-nanometer CMOS 10LP process. As a result, our customers can come to Chartered with confidence in achieving first-time silicon success at 65-nanometer as well as enjoying flexibility in their sourcing strategies."

"Synopsys has worked closely with the Common Platform foundries and ARM, utilizing the expertise of each company to deliver a complete, tested flow. Our ability to add important new capabilities such as support for advanced 65-nanometer

design rules and manufacturing-aware design tools is evidence of the cooperation among the companies," stated Glenn Dukes, vice president, Synopsys Professional Services. "Customers benefit in terms of improved design productivity. Since the flow is derived from the proven Pilot Design Environment and tuned for the Common Platform process technology and physical IP, project teams can quickly adopt it so they can focus on their design objectives rather than flow-related tasks."

Availability

The reference flow will be available at the end of July 2006 at no charge to Synopsys customers and may be obtained via Synopsys' SolvNet online support site at http://solvnet.synopsys.com/ . Supporting physical IP and technology files are also available from their respective suppliers.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at https://www.synopsys.com/ .

NOTE: Synopsys is a registered trademark of Synopsys, Inc. Astro, Hercules, and Milkyway are trademarks of Synopsys, Inc. All other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

Editorial Contacts:

Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Angela Costa
Edelman
650-429-2765
angela.costa@edelman.com

SOURCE: Synopsys, Inc.

CONTACT: Sheryl Gulizia of Synopsys, Inc., +1-650-584-8635, or sgulizia@synopsys.com; or Angela Costa of Edelman, +1-650-429-2765, or angela.costa@edelman.com, for Synopsys, Inc.

Web site: https://www.synopsys.com/