Virage Logic Standardizes on Synopsys' ESP for Memory Verification

ESP Boosts Verification Productivity by 2X for Memory Compilers

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, announced that Virage Logic Corporation (NASDAQ: VIRL), a leading provider of semiconductor IP platforms, has standardized on Synopsys' ESP memory equivalency checker for the embedded memory components of its IPrima™ Mobile semiconductor IP platform. ESP's unique symbolic simulation capabilities improve verification productivity by at least 2X over previous approaches. The increase in productivity enabled Virage Logic to trim the engineering time needed to complete functional verification of the circuits in its Area, Speed and Power (ASAP) Memory™ compilers from days to hours.

"ESP has a solid track record at Virage Logic, and we're now standardizing on it to verify the simulation models for our memories directly against the SPICE netlists," said Alex Shubat, chief technology officer and vice president of research and development at Virage Logic. "ESP provides a tremendous productivity boost to our verification team, enabling them to complete functional verification with less effort. In addition, ESP helps us debug the functionality in our models."

ESP is an equivalency checker for memories that compares a Verilog simulation model directly to an HSPICE® netlist. Its patented application of symbolic simulation and formal proof engines enables the functional verification of full-custom memories, macros and libraries used in today's complex ICs. ESP is ideally suited for verifying embedded memories in system-on-chip (SoC) designs.

"Virage Logic has long been a leader in providing differentiated embedded memory IP to the world's leading foundries, integrated device manufacturers and fabless customers worldwide," said Bijan Kiani, vice president of marketing at Synopsys. "Their standardization on ESP for memory IP is another example of ESP's ability to boost productivity and reduce time-to-results for memory verification."

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at https://www.synopsys.com/ .

NOTE: Synopsys and HSPICE are registered trademarks of Synopsys, Inc. All other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

SOURCE: Synopsys, Inc.

CONTACT: editorial, Nancy Renzullo of Synopsys, Inc., +1-650-584-1669,
or renzullo@synopsys.com; or Sarah Seifert of Edelman Public Relations,
+1-650-429-2776, or Sarah.seifert@edelman.com, for Synopsys, Inc.

Web site: https://www.synopsys.com/