# Synopsys Galaxy Test Solution Sets New Benchmark in Performance and Quality for Deep Submicron Designs

DFT Compiler and TetraMAX ATPG Double Performance and Halve Pattern Count

Synopsys Inc. (NASDAQ: SNPS), the world leader in semiconductor design software, today announced that the new releases of DFT Compiler™ and TetraMAX® ATPG -- key products in Synopsys' Galaxy™ Test Solution -- have improved design-for-test (DFT) performance and automatic test pattern generation (ATPG) performance and pattern count for deep submicron (DSM) designs. Customer benchmarks show two- to five-times improvement in DFT synthesis runtimes, and two- to three-times improvement in pattern count over the previous releases. This runtime improvement in Synopsys' DFT synthesis and ATPG products will help customers to significantly reduce overall test development time. Furthermore, the improvement in TetraMAX ATPG pattern count will help customers to maintain and improve product quality for rapidly growing design sizes in 0.13-micron processes and below, while remaining within test cost constraints.

"Synopsys Galaxy Test solutions are part of our standard design flow today," said Masaaki Yoshida, department manager of Technology Foundation Development Division, NEC Electronics Corporation. "The new releases of DFT Compiler and TetraMAX provide two- to three-times faster runtime and three times more compact at-speed test vectors on our latest two-to-six-million gate designs."

DFT Compiler and TetraMAX (version 2003.12) deliver enhanced capabilities that further improve productivity and quality of results. DFT Compiler's new Rapid Scan Synthesis Technology and new Unified Test DRC engine accelerate scan insertion and test design rule checking, enabling designers to complete design-for-test in significantly less time. Improved TetraMAX ATPG algorithms help optimize compressed pattern generation for multimillion-gate designs, simultaneously improving performance while reducing pattern count.

"Fast, accurate test pattern generation that is capable of excellent coverage of the ARM® cores is essential to our customers," said Tim Holden, EDA Relations manager, ARM. "Synopsys' newest version of TetraMAX enables us to reduce at-speed test pattern count by one half."

"Designers face the challenge of reducing their cost of test while improving product quality and meeting their time-to-market goals," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "Our latest improvements in DFT Compiler and TetraMAX help customers achieve these goals and demonstrate our continued commitment to maintaining industry leadership in our Galaxy Test offerings."

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at https://www.synopsys.com/ .

NOTE: Synopsys, the Synopsys logo and TetraMAX are registered trademarks of Synopsys, Inc., and DFT Compiler and Galaxy are trademarks of Synopsys. All other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

SOURCE: Synopsys, Inc.

CONTACT: editorial, Nancy Renzullo of Synopsys, Inc., +1-650-584-1669,
or renzullo@synopsys.com ; or Sarah Seifert of Edelman Public Relations,
+1-650-429-2776, or Sarah.seifert@edelman.com, for Synopsys, Inc.

Web site: https://www.synopsys.com/