Progate Tapes Out Advanced Mobile Communications Chip Using Synopsys IC Compiler

IC Compiler Enables 10 Percent Die-Size Shrink and 2X Faster Turnaround Time

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that Progate Group Corporation (PGC), one of the largest SoC/ASIC design service providers in Taiwan, has successfully taped out an advanced mobile communications chip using the Synopsys IC Compiler next-generation place-and-route solution. By utilizing the new optimizations in the IC Compiler tool, PGC designers were not only able to reduce the die size but also complete the design ahead of schedule.

"When it comes to mobile communications IC products, low unit cost and fast time-to-market are most critical to product success," said Albert Hu, CEO of PGC. "Thanks to the excellent implementation design technology and services from Synopsys, we were able to shrink the die size by 10 percent while completing the design within just one and a half months."

For this 1.5-million-gate, 130-nanometer design, PGC used Synopsys' IC Compiler solution to meet tight timing and performance goals. PGC also saw improvement in turnaround time consistent with other IC Compiler users who have reported 2X faster turnaround time compared to the previous-generation Physical Compiler/Astro solution, on average. Much of this productivity boost can be attributed to IC Compiler's Extended Physical Synthesis (XPS) technology that unifies optimizations across synthesis, placement, clock tree, and routing. In addition, PGC benefited from tighter correlation to Synopsys' golden Star-RCXT™ extraction tool and PrimeTime® sign-off technologies to accelerate the overall time to design closure. A long-time user of Synopsys physical implementation products, PGC is actively deploying IC Compiler into production for additional customer designs.

"The successful tapeout by PGC, including the very impressive reduction in die size, speaks to the strength of the IC Compiler solution," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "As PGC ramps up on their 90-nm designs, they can expect to benefit from the full complement of the technology innovations in IC Compiler, resulting in higher design performance and improved designer productivity."

About IC Compiler

IC Compiler is Synopsys' next-generation place-and-route solution. It provides superior results and faster time-to-results by extending physical synthesis to full place-and-route, and by enabling signoff-driven design closure. Current-generation solutions have a limited horizon because placement, clock tree, and routing are separate, disjointed operations. IC Compiler's Extended Physical Synthesis (XPS) technology breaks down the walls between these steps by extending physical synthesis to full place-and-route. IC Compiler has a unified, TCL-based architecture that implements innovations and harnesses some of the best Synopsys core technologies. It is a complete place-and-route system with everything necessary to do next-generation designs, including physical synthesis, placement, routing, timing, signal integrity (SI) optimization, power reduction, design-for-test (DFT), and yield optimization.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoC's). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at www.synopsys.com .

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