Renesas Adopts Synopsys' VCS Solution and VMM Methodology

Synopsys SystemVerilog Solution Used to Verify Next-Generation On-Chip Interconnect Infrastructure for Networking, Peripheral and Consumer Applications

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that Renesas Technology Corp., one of the world's leading semiconductor system solutions providers for mobile, automotive and PC/AV (Audio Visual) markets, has adopted the VCS® functional verification solution for the development of complex systems-on-chip (SoC). In addition, Renesas has adopted the VMM methodology, as defined in the Verification Methodology Manual (VMM) for SystemVerilog, for the creation of advanced SoC verification environments. Renesas used the VCS solution with the VMM methodology to verify its critical SuperHyway bus on-chip interconnect infrastructure.

"We have adopted VCS, SystemVerilog and the VMM methodology for our next generation of advanced SoC verification environments," said Kazunobu Morimoto, group manager, System Level Design and Verification Technology Department at Renesas. "SystemVerilog and the VMM methodology have proven easy to adopt and deploy with the VCS solution, and will enable significant improvements in verification productivity in our Soc designs using the SuperHyway bus."

Improving Productivity with VCS and VMM Methodology

The SuperHyway bus is a VSIA/VCI compliant on-chip interconnect infrastructure designed to give developers a scalable high-bandwidth, low-latency interconnect. Renesas needed to improve the productivity and predictability of the SuperHyway bus verification environment to keep up with growing demand for new system components. Their new environment needed to reuse legacy tests, enable detailed verification-progress tracking using coverage, and allow for easy addition, modification and maintenance.

Over a period of nine months, Renesas engineers learned the SystemVerilog language and the VMM methodology and built a comprehensive verification environment for the SuperHyway bus running in the VCS solution. Key components of the environment included assertion-based protocol checkers, transaction checkers and scoreboards, transaction-level initiator and target models, coverage descriptions and a legacy test interface. All components were built using SystemVerilog and followed the VMM methodology. Renesas realized many benefits, including higher verification productivity with the transaction- level modeling and constrained-random, coverage-driven capabilities of the VMM methodology, as well as the ability to easily reuse legacy tests. In addition, the verification code base for the new environment was one-third smaller than the legacy environment and was easier to maintain and extend for new projects due to the VMM methodology's clean, layered architecture.

"Renesas has proven that SystemVerilog and the VMM methodology can greatly improve verification productivity, while being easy to adopt and deploy," said George Zafiropoulos, vice president of Marketing, Verification Group at Synopsys, Inc. "The VCS solution's superior support for SystemVerilog and the VMM methodology make it the preferred choice for companies looking to move to higher levels of verification productivity and predictability."

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http:/www.synopsys.com .

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