Synopsys Introduces Validated USB 2.0 nanoPHY IP for TSMC's Nexsys(SM) 90-LP Process

Silicon-Proven DesignWare PHY Cuts Power and Size in Half for Portable, High-Volume Consumer SoCs

PRNewswire-FirstCall
MOUNTAIN VIEW, Calif.

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced the immediate availability of the DesignWare® USB 2.0 nanoPHY intellectual property (IP) for Taiwan Semiconductor Manufacturing Company's (TSMC's) Nexsys 90-nanometer (nm) low-power (LP) process. The DesignWare USB 2.0 nanoPHY IP is Synopsys' next-generation USB 2.0 mixed-signal PHY targeting low-power and consumer applications. The DesignWare nanoPHY IP for TSMC's 90- nm process was developed with TSMC's proven Nexsys standard cell libraries, which TSMC designed according to their 90-nm design-for-manufacturing rules. This gives system-on-chip (SoC) designers a proven PHY, which lowers risk and enables predictable results.

The DesignWare USB 2.0 nanoPHY IP is Hi-Speed USB logo-certified and requires half the power and die area compared to previous-generation solutions. Ideal for applications requiring longer battery life and lower silicon cost, the DesignWare nanoPHY IP will benefit next-generation handheld game machines, feature-rich smart phones, digital cameras and portable audio/video players. A single-port, on-the-go (OTG) configuration takes up only 0.6 square millimeter (mm2) of area and consumes less than 30mA of current during high-speed data transmission. The DesignWare nanoPHY IP is also tunable for optimal yield by enabling adjustments in key PHY performance parameters to address effects related to process variation as well as package- or board-level issues.

"TSMC and Synopsys have worked together to ensure that designers have access to quality USB PHYs for our leading 90-nm processes," said Ed Wan, senior director of Design Service Marketing at TSMC. "The combination of DesignWare USB 2.0 nanoPHY IP and TSMC's Nexsys standard cell libraries provide the industry with low-power, cost-effective USB IP."

"As the leader in USB IP, we collaborate with TSMC to deliver IP solutions that enable our customers to meet critical market windows," said Guri Stark, vice president of Marketing for the Solutions Group at Synopsys. "Our complete and silicon-proven USB IP product line, including PHYs, digital controller cores and verification IP, enables designers to integrate high-quality USB IP into their next-generation portable and consumer electronic applications."

Availability

The DesignWare USB 2.0 nanoPHY IP is available today in TSMC's 90-LP process. The complete set of TSMC Nexsys standard cell libraries is available today at no additional cost to DesignWare Library licensees. The libraries can be downloaded at https://www.synopsys.com/community/partners/tsmc.html .

About DesignWare Mixed-Signal IP

Synopsys enables designers to quickly integrate analog Mixed-Signal IP (MSIP) into next-generation SoCs with a comprehensive portfolio of high- performance PHYs for the PCI Express, SATA, XAUI, and USB protocols. In addition, the MSIP offering also includes a complete suite of I/O Libraries. Available for industry-leading processes, DesignWare Mixed-Signal IP meets the needs of today's high-speed designs for the networking, storage, computing and consumer electronics markets. The DesignWare MSIP offering is complemented by a comprehensive suite of digital controller cores and verification IP to provide chip developers with a complete solution for SoC integration. Each MSIP can be licensed individually, on a fee-per-project basis or customers can opt for the Volume Purchase Agreement, which enables them to license all the MSIP in one simple agreement.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

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