New SystemVerilog Book Helps Engineers Master Assertion-Based Verification

VhdlCohen Publishes SystemVerilog Assertions Handbook

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VhdlCohen Publishing, a verification service provider, today announced the immediate availability of a new book, SystemVerilog Assertions Handbook, a guide to using SystemVerilog Assertions for formal and dynamic verification. The book is co-authored by Ben Cohen, a well-known consultant and author of several technical books addressing the effective use of Verilog and VHDL for logic design and verification; Srinivasan Venkataramanan, Verification Solutions Applications Engineer at Synopsys, Inc.; and Ajeetha Kumari, an independent consultant in the field of design and verification. The book is intended for engineers involved in the increasingly important task of verifying the functionality of complex digital electronic circuits. It presents Assertion-Based Verification methodology concepts using the SystemVerilog language.

"The SystemVerilog Assertions Handbook provides a clear presentation of concepts with practical examples and appropriate usage of the SystemVerilog language features," said Surrendra Dudani, Synopsys Scientist and a member of the Accellera SystemVerilog Technical Committee. "It is a much-needed guide to more fully capitalize on the many benefits offered by SystemVerilog Assertions." The Accellera SystemVerilog Technical Committee is responsible for maintaining and extending the SystemVerilog language for assertion support.

"This book introduces the concepts and importance of assertion-based verification, and then goes into great depth on how to write both simple and complex assertions," said Stuart Sutherland, consultant for Sutherland HDL, Inc. and author of the book SystemVerilog for Design. "Hundreds of examples illustrate the proper usage of SystemVerilog assertions. These examples serve as a cookbook of assertions that can be applied to a variety of designs."

The SystemVerilog Assertions Handbook explains the various syntax and nuances of the language in an easy-to-read manner with many examples. Using a synchronous, first in, first out (FIFO) design example, the authors demonstrate how assertions are used throughout all phases of the design process. Phases covered include system-level definition, architectural and verification plans, RTL and testbench designs, and formal verification concepts.

"The authors have created an excellent source for mastering the art of assertion-based specification," said Harry D. Foster, chief methodologist at Jasper Design Automation and chairman of the Accellera Formal Verification Technical Committee. "They provide clear explanations and relevant examples throughout the book, including actual results using several commercial electronic design automation software tools."

The SystemVerilog Assertions Handbook for formal and dynamic verification is available immediately. To find out more about the book or to order it online, visit www.abv-sva.org. A free copy of the book will be provided to eligible attendees of the Design and Verification Conference (DVCon) tutorial entitled "SystemVerilog Assertions: Best Practices for Functional Verification," held on February 14th, in San Jose, California. To register for the tutorial, visit www.dvcon.com.

About VhdlCohen Publishing

VhdlCohen Publishing provides verification education and services and has teamed with Stuart Sutherland of Sutherland HDL, Inc., and a member of the IEEE P1800 SystemVerilog Working Group, to provide training of SystemVerilog assertions. VhdlCohen was founded in 2000 in Palos Verdes Peninsula, California. More information can be found at www.abv-sva.org.

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