

Synopsys' 14th EDA Interoperability Developers' Forum Features Widest Range of Industry Initiatives

Synopsys Extends Popular Liberty and SDC Open Source Formats

Synopsys, Inc. (NASDAQ: SNPS), the world leader in semiconductor design software, today announced that the fourteenth electronic design automation (EDA) Interoperability Developers' Forum will be held on October 21, 2004 in Santa Clara, CA. This open forum presents the widest range of EDA initiatives and standards ever in the event's seven-year history. Synopsys will also announce significant extensions to its Liberty™ library and Synopsys Design Constraints (SDC) open source formats.

The Forum's keynote address, entitled, "The Next Big IC Design Discontinuity," will be delivered by University of California, Berkeley Professor A. Richard Newton, dean of the College of Engineering. In 2004, Dr. Newton was named to the National Academy of Engineers and, in 2003, won the Phil Kaufman Award, the EDA Consortium's highest recognition.

The Forum will also present two exciting panels: "The Business of Standards" moderated by Peggy Aycineya, and "Software Piracy and Export Control" moderated by Mike Santarini. Two afternoon tracks will also be available: the Low-Power Forum and the SystemVerilog Developers' Forum. The Low-Power forum offers a deep technical discussion on the elements of Energy Efficient SoC Design. Several partners will present how their solutions facilitate achieving low power SoCs for the market. The SystemVerilog Developers' Forum will feature presentations on SystemVerilog testbench constructs, as well as designer and EDA vendor perspectives on the language.

At the forum, Synopsys will unveil extensions to the Liberty library format to model variations such as miller capacitance and IR-drop that become significant at process geometries below 90-nm. Using these library extensions allows Synopsys' PrimeTime® to deliver high accuracy post-layout RC delay calculation within 2 percent of HSPICE®.

Synopsys will also announce the expansion of the SDC format to include information for cross-referencing a synthesized netlist to its RTL source. Changes made during design implementation, such as name and register optimizations, can be captured in these new SDC constructs to improve interoperability, performance and productivity across implementation and verification tools.

"The Interoperability Developers' Forum underscores the importance that Synopsys places on EDA interoperability -- now and for the future," said Rich Goldman, vice president of Strategic Market Development at Synopsys. "As an industry leader in this arena, we find tremendous value in the opportunity to exchange information and ideas with our customers and partners regarding tool interoperability. As a result, the EDA industry is able to successfully deliver the solutions and initiatives our customers and partners require."

Registration and About the EDA Interoperability Developers' Forum

This forum provides EDA vendors and their customers an opportunity to exchange information and ideas on EDA tool interoperability including new interface technologies, future enhancements, upcoming news, and successes. For more information and to register, visit <https://www.synopsys.com/devforum/oct2004>.

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at <https://www.synopsys.com/>.

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