Synopsys 2006.06 Release of DesignWare Library Reduces Area and Delay in IC Designs

Synopsys Expands DesignWare Library With More Than 20 New IP Components

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that it has expanded its DesignWare® Library intellectual property (IP) by adding more than 20 new components. The additions include 10 floating point operations and four complex datapath functions. When used with Synopsys Design Compiler® synthesis tool, DesignWare Library yields an average reduction of 6% in area and 10% in delay for designs with 20% or greater datapath content. These improvements help reduce design time and risk and improve quality of results (QoR), helping ensure predictable success for complex systems-on-chip (SoC) designs.

New datapath components added to the DesignWare Library, including the floating point family and functions such as blend and saturate, are particularly important because the percentage of datapath content is steadily rising for most computationally intensive designs. In chips for graphics and multimedia processor applications, greater than 50 percent of the die area is devoted to datapath. The new floating point operations are designed for datapath optimization in these important markets.

The DesignWare Library datapath optimizations occur automatically within Synopsys Design Compiler RTL synthesis and concurrently with other logic optimizations, and use the same timing engine to take advantage of the full timing context of the surrounding logic. Correct results can be easily verified using Synopsys Formality® equivalency checking tool.

"DesignWare Library datapath optimizations give our customers better QoR with every new release," said Guri Stark, vice president of Marketing for the Solutions Group at Synopsys. "The significant additions of more than 20 new datapath components, such as the floating point sum3, enable customers in computationally intensive markets such as graphics and multimedia to achieve higher accuracy while reducing design area. More than 25,000 DesignWare Library users can now access this new IP within their existing synthesis flow."

Availability

The new DesignWare Library datapath components and optimizations are available in the 2006.06 release, which is available now to DesignWare Library licensees. For more information on datapath components visit: http://www.synopsys.com/dw/buildingblock.php.

About DesignWare Library

The DesignWare Library contains the principal intellectual property ingredients for design and verification including high-speed datapath components, AMBA On-Chip Bus, microcontrollers (8051, 6811) memory portfolio (memory controller, memory BIST, memory building blocks), verification IP of standard bus and I/Os (PCI, PCI-X, USB, SATA, XAUI, Ethernet), design views of popular Star IP models, board verification IP and Foundry Libraries. All DesignWare Library elements are available under one license with no additional costs, per use fees, or royalties. For more information on DesignWare IP, visit: http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

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